CMOS 200 MSPS 14-Bit Quadrature Digital Upconverter

AD9857

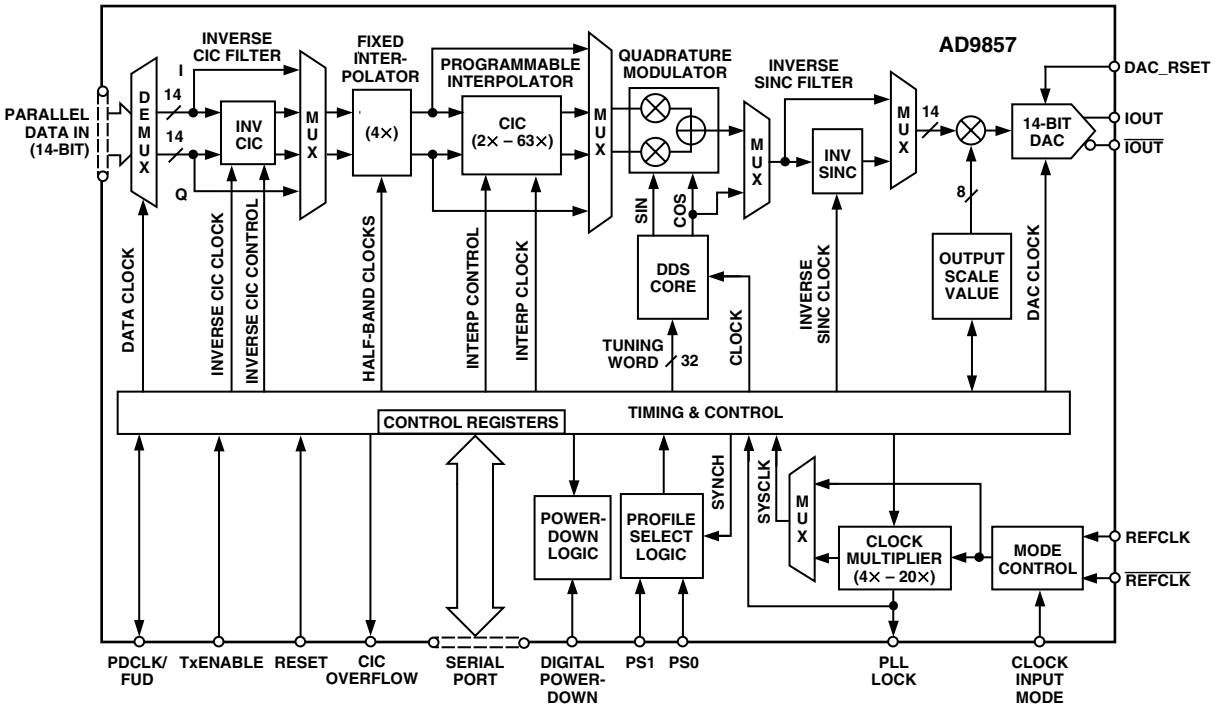
FEATURES
200 MHz Internal Clock Rate
14-Bit Data Path
Excellent Dynamic Performance
80 dB SFDR @ 65 MHz (±100 kHz) A_{OUT}
4×–20× Programmable Reference Clock Multiplier
Reference Clock Multiplier PLL Lock Detect Indicator
Internal 32-Bit Quadrature DDS
FSK Capability
8-Bit Output Amplitude Control
Single-Pin Power-Down Function
Four Programmable, Pin-Selectable Signal "Profiles"
SIN(x)/x Correction (Inverse SINC Function)
Simplified Control Interface
10 MHz Serial, 2- or 3-Wire SPI-Compatible
3.3 V Single Supply
Single-Ended or Differential Input Reference Clock
80-Lead LQFP Surface-Mount Packaging
Three Modes of Operation
Quadrature Modulator Mode
Single-Tone Mode
Interpolating DAC Mode

APPLICATIONS
HFC Data, Telephony, and Video Modems
Wireless Base Station
Agile, L.O. Frequency Synthesis
Broadband Communications

GENERAL DESCRIPTION

The AD9857 integrates a high-speed direct-digital synthesizer (DDS), a high-performance, high-speed 14-bit digital-to -analog converter (DAC), clock multiplier circuitry, digital filters, and other

FUNCTIONAL BLOCK DIAGRAM



REV.0

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AD9857–SPECIFICATIONS

(V_S = 3.3 V ± 5%, R_{SET} = 1.96 kΩ, External reference clock frequency = 10 MHz with REFCLK Multiplier enabled at 20 ×).

Parameter	Temp	Level	Min	Typ	Max	Unit	Test	AD9857	
REF CLOCK INPUT CHARACTERISTICS									
Frequency Range									
REFCLK Multiplier Disabled		Full	VI	1200		MHz			
REFCLK Multiplier Enabled at 4 ×		Full	VI	150		MHz			
REFCLK Multiplier Enabled at 20 ×		Full	VI	110		MHz			
Input Capacitance	25		°C	V	3	pF			
Input Impedance	25		°C	V	100	M			Ω
Duty Cycle	25		°C	V	50	%			
Duty Cycle with REFCLK Multiplier Enabled, Voltage Mode	25		°C	V	35	65%			
Duty Cycle, Current Mode	25		°C	V	50	%			
DAC OUTPUT CHARACTERISTICS									
Resolution								14Bits	
Full-Scale Output Current	5	10	20			mA			
Gain Error	25		°C	I	8.5	0% FS			
Output Offset	25		°C	I	2				µA
Differential Nonlinearity	25		°C	V	1.6	LSB			
Integral Nonlinearity	25		°C	V	2	LSB			
Output Capacitance	25		°C	V	5	pF			
Residual Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}									
REFCLK Multiplier Enabled at 20 ×	25		°C	V	–107	dBc/Hz			
REFCLK Multiplier at 4 ×	25		°C	V	–123	dBc/Hz			
REFCLK Multiplier Disabled	25		°C	V	–145	dBc/Hz			
Voltage Compliance Range	25		°C	I	–0.5	+1.0V			
Wideband SFDR									
1 MHz–20 MHz Analog Out	25		°C	V	–75	dBc			
20 MHz–40 MHz Analog Out	25		°C	V	–65	dBc			
40 MHz–60 MHz Analog Out	25		°C	V	–62	dBc			
60 MHz–80 MHz Analog Out	25		°C	V	–60	dBc			
Narrowband SFDR									
10 MHz Analog Out (±1 MHz)	25		°C	V	–87	dBc			
10 MHz Analog Out (±250 kHz)	25		°C	V	–88	dBc			
10 MHz Analog Out (±50 kHz)	25		°C	V	–92	dBc			
10 MHz Analog Out (±10 kHz)	25		°C	V	–94	dBc			
65 MHz Analog Out (±1 MHz)	25		°C	V	–86	dBc			
65 MHz Analog Out (±250 kHz)	25		°C	V	–86	dBc			
65 MHz Analog Out (±50 kHz)	25		°C	V	–86	dBc			
65 MHz Analog Out (±10 kHz)	25		°C	V	–88	dBc			
80 MHz Analog Out (±1 MHz)	25		°C	V	–85	dBc			
80 MHz Analog Out (±250 kHz)	25		°C	V	–85	dBc			
80 MHz Analog Out (±50 kHz)	25		°C	V	–85	dBc			
80 MHz Analog Out (±10 kHz)	25		°C	V	–86	dBc			
MODULATOR CHARACTERISTICS (65 MHz A_{OUT}) (Input Data: 2.5 MS/s, QPSK, 4 × Oversampled, INV SINC ON, INV CIC ON))									
I/Q Offset	25		°C	IV	55	65dB			
Error Vector Magnitude	25		°C	IV	0.41	%			
INVERSE SINC FILTER (Variation in Gain from DC to 80 MHz, Inverse SINC Filter ON	25		°C	V				±0.1dB	
SPURIOUS POWER (Off Channel, Measured in Equivalent Bandwidth), Full-Scale Output									
6.4 MHz Bandwidth	25		°C	IV	–65	dBc			
3.2 MHz Bandwidth	25		°C	IV	–67	dBc			
1.6 MHz Bandwidth	25		°C	IV	–69	dBc			
0.8 MHz Bandwidth	25		°C	IV	–69	dBc			
0.4 MHz Bandwidth	25		°C	IV	–70	dBc			
0.2 MHz Bandwidth	25		°		72				

Parameter	Temp	Level	Min	Typ	Max	Unit	Test	AD9857	
SPURIOUS POWER (Off Channel, Measured in Equivalent Bandwidth), Output Attenuated 18 dB Relative to Full Scale									
6.4 MHz Bandwidth	25	°C		IV	–51	dBc			
3.2 MHz Bandwidth	25	°C		IV	–54	dBc			
1.6 MHz Bandwidth	25	°C		IV	–56	dBc			
0.8 MHz Bandwidth	25	°C		IV	–59	dBc			
0.4 MHz Bandwidth	25	°C		IV	–62	dBc			
0.2 MHz Bandwidth	25	°C		IV	–63	dBc			
TIMING CHARACTERISTICS									
Serial Control Bus									
Maximum Frequency	25	°C		I	10	MHz			
Minimum Clock Pulsewidth Low (t_{PWL})	25	°C		I	30	ns			
Minimum Clock Pulsewidth High (t_{PWH})	25	°C		I	30	ns			
Maximum Clock Rise/Fall Time	25	°C		I	1	ms			
Minimum Data Setup Time (t_{DS})	25	°C		I	30	ns			
Minimum Data Hold Time (t_{DH})	25	°C		I	0	ns			
Maximum Data Valid Time (t_{DV})	25	°C		I	35	ns			
Wake-Up Time[1]	25	°C		I	1	ms			
Minimum RESET Pulsewidth High (t_{RH})	25	°C		I	5	SYSCLK			[2] Cycles
Minimum $\overline{CS}$ Setup Time	25	°C		I	40	ns			
CMOS LOGIC INPUTS									
Logic “1” Voltage	25	°C		I	2.0	V			
Logic “0” Voltage	25	°C		I	0.8	V			
Logic “1” Current	25	°C		I	5				µA
Logic “0” Current	25	°C		I	5				µA
Input Capacitance	25	°C		V	3	pF			
CMOS LOGIC OUTPUTS (1 mA LOAD)									
Logic “1” Voltage	25	°C		I	2.7	mA			
Logic “0” Voltage	25	°C		I	0.4	mA			
POWER SUPPLY V_S CURRENT[3] (All Power Specs at V_{DD} = 3.3 V, 25°C, REFCLK = 200 MHz)									
Full Operating Conditions	25	°C		I	615	mA			
160 MHz Clock (×16)	25	°C		I	515	mA			
120 MHz Clock (×12)	25	°C		I	400	mA			
Burst Operation (25%)	25	°C		I	450	mA			
Single-Tone Mode	25	°C		I	310	mA			
Power-Down Mode	25	°C		I	80	mA			
Full-Sleep Mode	25	°C		I	13.5	mA			

NOTES

[1]Wake-Up Time refers to recovery from Full Sleep Mode. The longest time required is for the Reference Clock Multiplier PLL to lock up (if it is being used). The Wake-Up Time assumes that there is no capacitor on DAC_BP, and that the recommended PLL loop filter values are used. The state of the Reference Clock Multiplier lock can be determined by observing the signal on the PLL_LOCK pin.

[2]SYSCLK refers to the actual clock frequency used on-chip by the AD9857. If the Reference Clock Multiplier is used to multiply the external reference frequency, the SYSCLK frequency is the external frequency multiplied by the Reference Clock Multiplier multiplication factor. If the Reference Clock Multiplier is not used, the SYSCLK frequency is the same as the external REFCLK frequency.

[3]CIC = 2, INV SINC ON, FTW = 40%, PLL OFF, Auto Power-Down Between Burst On, TxENABLE Duty Cycle = 25%.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS *

Maximum Junction Temperature . . . . . .150 °C
V_S . . . . . .4 V
Digital Input Voltage . . . . . .–0.7 V to +V s
Digital Output Current . . . . . .5 mA
Storage Temperature . . . . . .–65 °C to +150°C
Operating Temperature . . . . . .–40 °C to +85°C
Lead Temperature (Soldering 10 sec) . . . . . .300 °C
θ_{JA} . . . . . .35 °C/W
θ_{JC} . . . . . .16 °C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I–100% Production Tested.

III–Sample Tested Only.

IV–Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI–Devices are 100% production tested at 25 °C and guaranteed by design and characterization testing for industrial operating temperature range.

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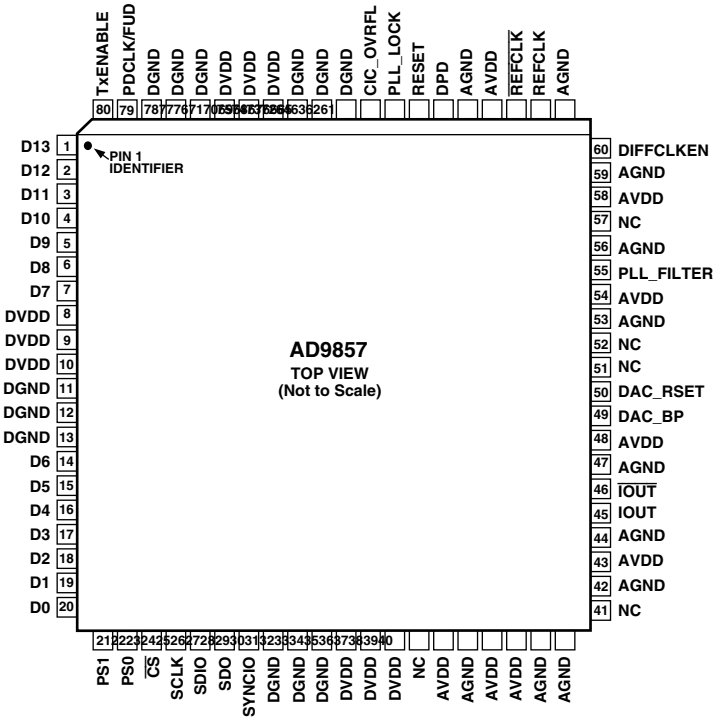
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	
AD9857AST	–40 °C to +85°C	Quad Flatpack	ST-80	
AD9857/PCB	25 °C	Evaluation Board		

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9857 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	I/O	Pin Function
20–14, 7–1	D0–D6, D7–D13	I	14-Bit Parallel Data Bus for I and Q Data. The required numeric format is two's complement with D13 as the sign bit and D12–D0 as the magnitude bits. Alternating 14-bit words are demultiplexed onto the I and Q data pathways (except when operating in the Interpolating DAC Mode, in which case every word is routed onto the I data path). When the TxENABLE pin is asserted high, the next accepted word is presumed to be I data, the next Q data, and so forth.
8–10, 31–33, 73–75	DVDD		3.3 V Digital Power Pin(s).
11–13, 28–30, 70–72, 76–78	DGND		Digital Ground Pin(s).
21	PS1	I	Profile Select Pin 1. The LSB of the two profile select pins. In conjunction with PS0, selects one of four profile configurations.
22	PS0	I	Profile Select Pin 0. The MSB of the two profile select pins. In conjunction with P1, selects one of four profile configurations.
23	$\overline{CS}$	I	Serial Port Chip Select Pin. An active low signal that allows multiple devices to operate on a single serial bus.
24	SCLK	I	Serial Port Data Clock Pin. The serial data CLOCK for the Serial Port.
25	SDIO	I/O	Serial Port Input/Output Data Pin. Bidirectional serial DATA pin for the Serial Port. This pin can be programmed to operate as a serial *input only* pin, via a control register bit 00h<7>. The default state is bidirectional.
26	SDO	O	Serial Port Output Data Pin. This pin serves as the serial data output pin when the SDIO pin is configured for serial input only mode. The default state is three-state.
27	SYNCIO	I	Serial Port Synchronization Pin. Synchronizes the serial port without affecting the programmable register contents. This is an active high input that aborts the current serial communication cycle.
34, 41, 51, 52, 57	NC		No Connect.
35, 37, 38, 43, 48, 54, 58, 64	AVDD		3.3 V Analog Power Pin(s).
36, 39, 40, 42, 44, 47, 53, 56, 59, 61, 65	AGND		Analog Ground Pin(s).
45	IOUT	O	DAC Output Pin. Normal DAC output current (analog).
46	$\overline{IOUT}$	O	DAC Complementary Output Pin. Complementary DAC output current (analog).
49	DAC_BP		DAC Reference Bypass. Normally not used.
50	DAC_RSET	I	DAC Current Set Pin. Sets DAC reference current
55	PLL_FILTER	O	PLL Filter. R-C network for PLL Filter.
60	DIFFCLKEN	I	Clock Mode Select Pin. A logic high on this pin selects DIFFERENTIAL REFCLK input mode. A logic low selects the SINGLE-ENDED REFCLK input mode.
62	REFCLK	I	Reference Clock Pin. In single-ended Clock Mode, this pin is the Reference Clock input. In differential Clock Mode, this pin is the positive clock input.
63	$\overline{REFCLK}$	I	Inverted Reference Clock Pin. In differential Clock Mode, this pin is the negative clock input.
66	DPD	I	Digital Power-Down Pin. Assertion of this pin shuts down the digital sections of the device to conserve power. However, if selected, the PLL remains operational.
67	RESET	I	Hardware RESET Pin. An active high input that forces the device into a predefined state.
68	PLL_LOCK	O	PLL Lock Pin. Active high output signifying, in real time, when PLL is in "lock" state.
69	CIC_OVRFL	O	CIC Overflow Pin. Activity on this pin indicates that the CIC filters are in "overflow" state. This pin is normally "low" unless a CIC overflow occurs.
79	PDCLK/FUD	I/O	Parallel Data Clock/Frequency Update Pin. When not in Single-Tone Mode, this pin is an output signal that should be used as a clock to synchronize the acceptance of the 14-bit parallel data words on Pins D13–D0. In Single-Tone Mode, this pin is an input signal that synchronizes the transfer of a changed frequency tuning word (FTW) in the active profile (PSx) to the accumulator (FUD = Frequency Update signal). When profiles are changed by means of the PS–PS1 pins, the FUD does not have to be asserted to make the FTW active.
80	TxENABLE	I	When TxENABLE is asserted, the device processes the data through the I and Q data pathways; otherwise 0s are internally substituted for the I and Q data entering the signal path. The first data word accepted when the TxENABLE is asserted high is treated as I data, the next data word is Q data, and so forth.

Typical Modulated Output Spectral Plots

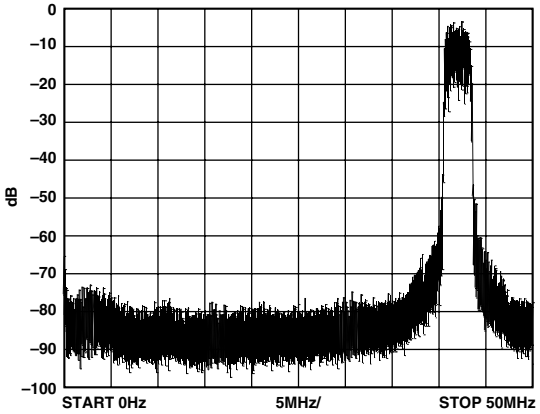


Figure 1. QPSK at 42 MHz and 5.12 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC Interpolation Rate = 3, 4× Oversampled Data

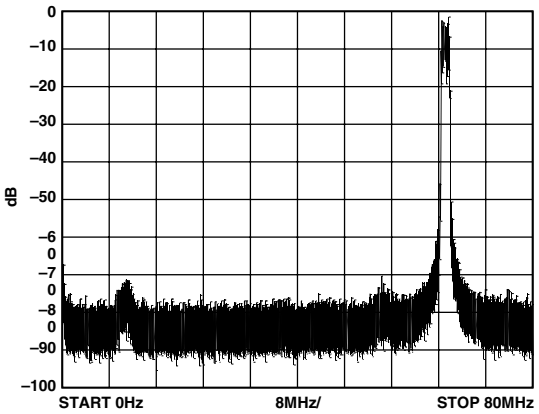


Figure 3. 16-QAM at 65 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC Interpolation Rate = 9, 4× Oversampled Data

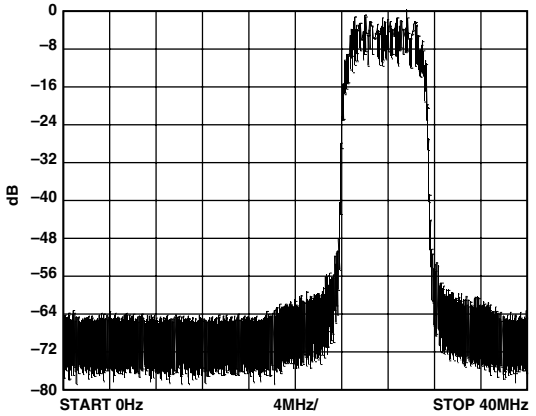


Figure 2. 64-QAM at 28 MHz and 6 MS/s; 36 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 3× Oversampled Data

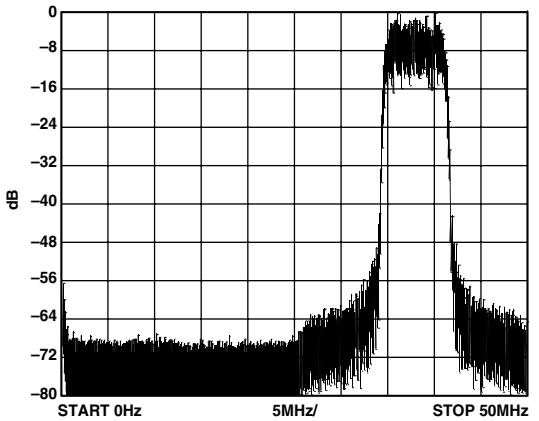


Figure 4. 256-QAM at 38 MHz and 6 MS/s; 48 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 4× Oversampled Data

Typical Single-Tone Output Spectral Plots

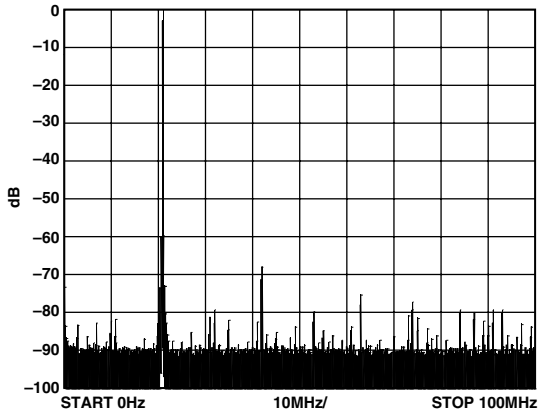


Figure 5. 21 MHz Single-Tone Output

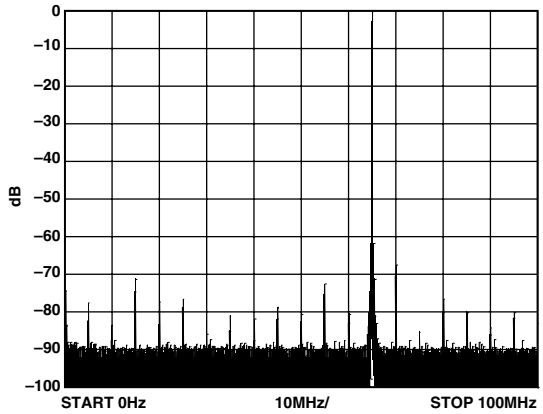


Figure 6. 65 MHz Single-Tone Output

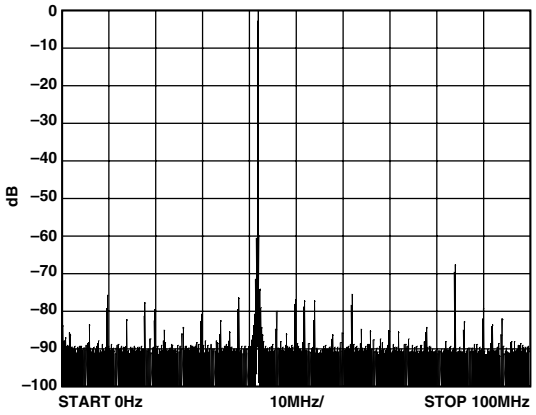


Figure 7. 42 MHz Single-Tone Output

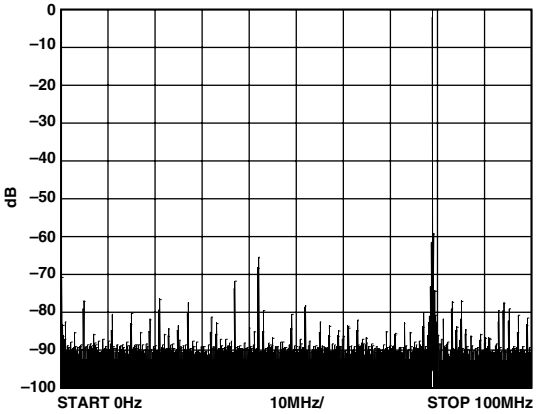


Figure 8. 79 MHz Single-Tone Output

Typical Narrowband SFDR Spectral Plots

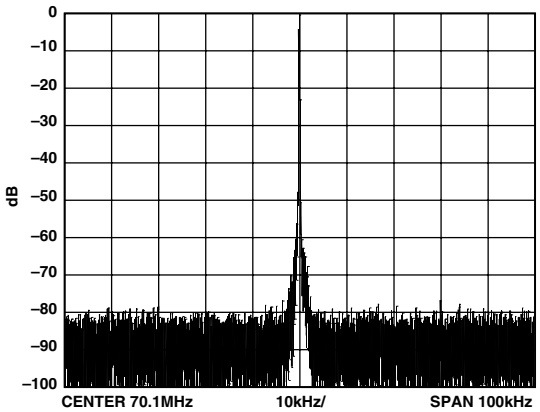


Figure 9. 70.1 MHz Narrowband SFDR, 10 MHz External Clock with REFCLK Multiplier = 203

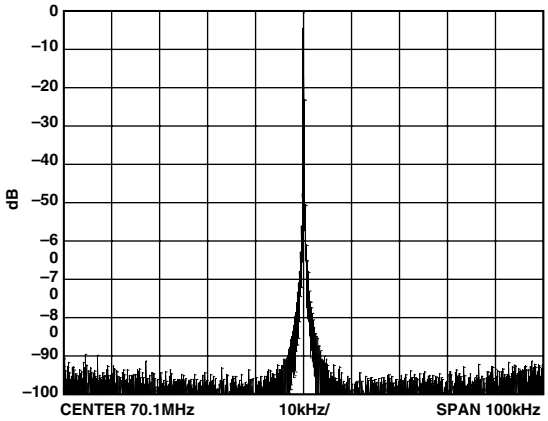


Figure 10. 70.1 MHz Narrowband SFDR, 200 MHz External Clock with REFCLK Multiplier Disabled

Typical Plots of Output Constellations

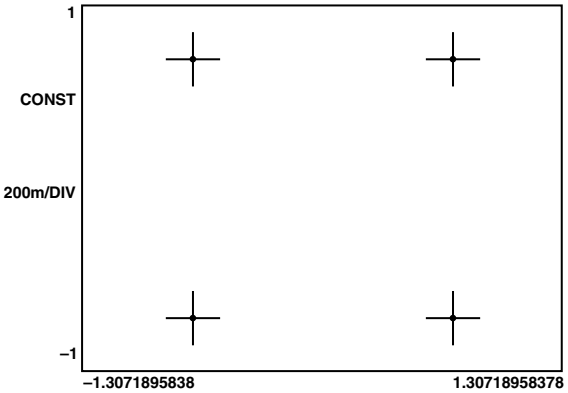


Figure 11. QPSK, 65 MHz, 2.56 MS/s

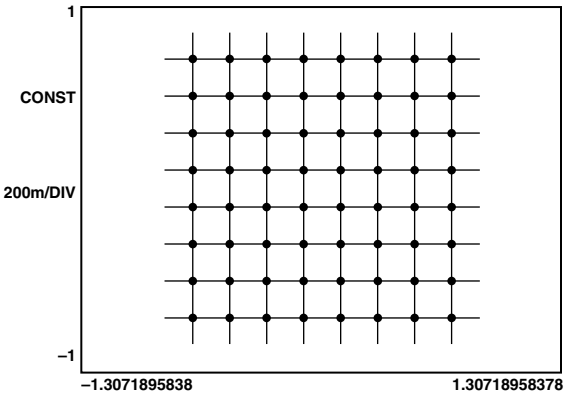


Figure 12. 64-QAM, 42 MHz, 6 MS/s

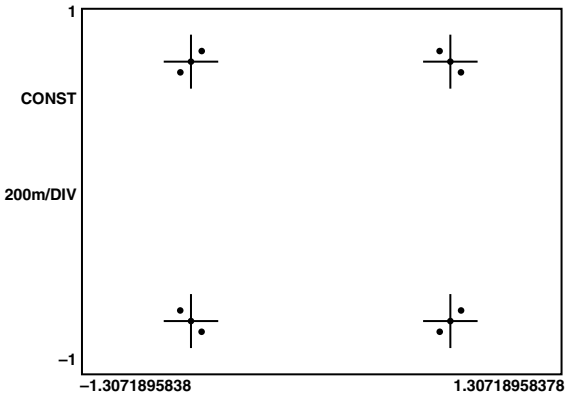


Figure 13. GMSK Modulation, 13 MS/s

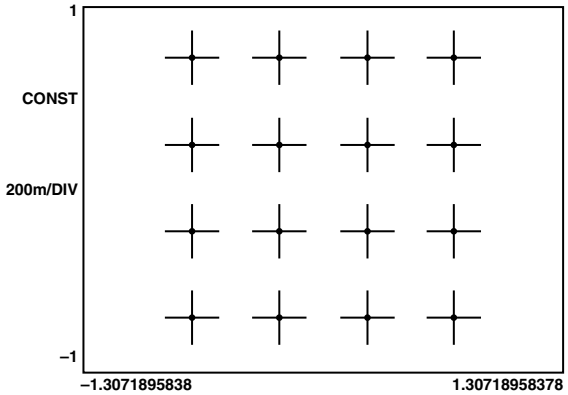


Figure 14. 16-QAM, 65 MHz, 2.56 MS/s

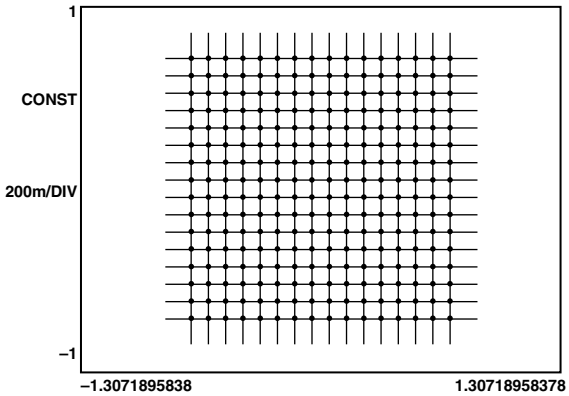


Figure 15. 256-QAM, 42 MHz, 6 MS/s

MODES OF OPERATION

The AD9857 has three operating modes:

- Quadrature Modulation Mode (Default)
- Single-Tone Mode
- Interpolating DAC Mode

Mode selection is accomplished by programming a control register via the Serial Port. The Inverse SINC filter and output scale multiplier are available in all three modes.

Quadrature Modulation Mode

In Quadrature Modulation Mode both the I and Q data paths are active. A block diagram of the AD9857 operating in the Quadrature Modulation Mode is shown in Figure 16.

In Quadrature Modulation Mode, the PDCLK/FUD pin is an output and functions as the Parallel Data Clock (PDCLK), which serves to synchronize the input of data to the AD9857. In this mode, the input data must be synchronized with the rising edge of PDCLK. The PDCLK operates at *twice* the rate of either the I or Q data path. This is because of the fact that the I and Q data must be presented to the parallel port as two 14-bit words multiplexed in time. One I word and one Q word together comprise one internal *sample*. Each sample is propagated along the internal data pathway in parallel fashion.

The DDS Core provides a quadrature (sin and cos) local oscillator signal to the quadrature modulator, where the I and Q data are multiplied by the respective phase of the carrier and summed together, to produce a quadrature-modulated data stream.

All of this occurs in the digital domain, and only then is the digital data stream applied to the 14-bit DAC to become the quadrature-modulated analog output signal.

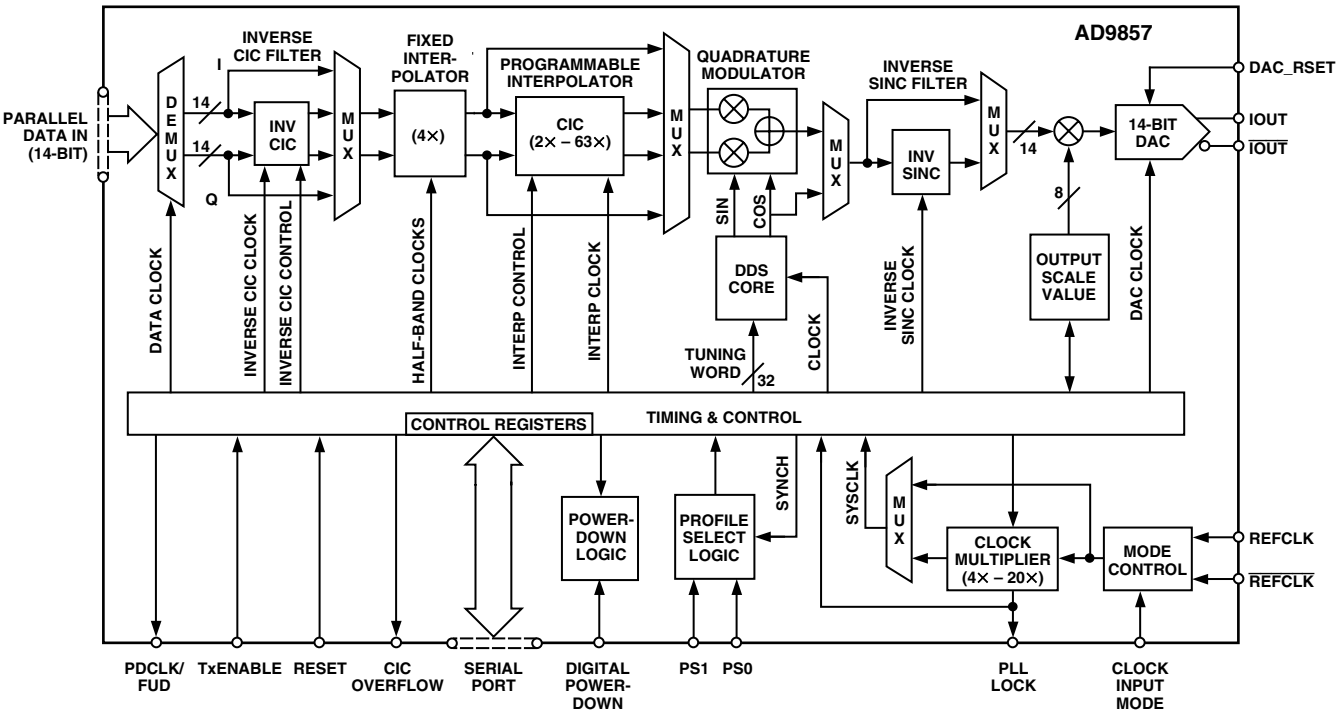


Figure 16. Quadrature Modulation Mode

Single-Tone Mode

A block diagram of the AD9857 operating in the Single-Tone Mode is shown in Figure 17. In the Single-Tone Mode both the I and Q data paths are disabled from the 14-bit Parallel Data Port up to and including the modulator. The PDCLK/FUD pin is an input and functions as a Frequency Update (FUD) control signal. This is necessary because the frequency tuning word is programmed via the asynchronous serial port. The FUD signal causes the new frequency tuning word to become active.

In Single-Tone Mode, the cosine portion of the DDS serves as the signal source. The output signal consists of a single frequency as determined by the tuning word stored in the appropriate control register, per each profile.

In the Single-Tone Mode, no 14-bit parallel data is applied to the AD9857. The internal DDS core is used to produce a single frequency signal according to the tuning word. The single-tone signal then moves toward the output, where the Inverse SINC filter and the output scaling can be applied. Finally, the digital single-tone signal is converted to the analog domain by the 14-bit DAC.

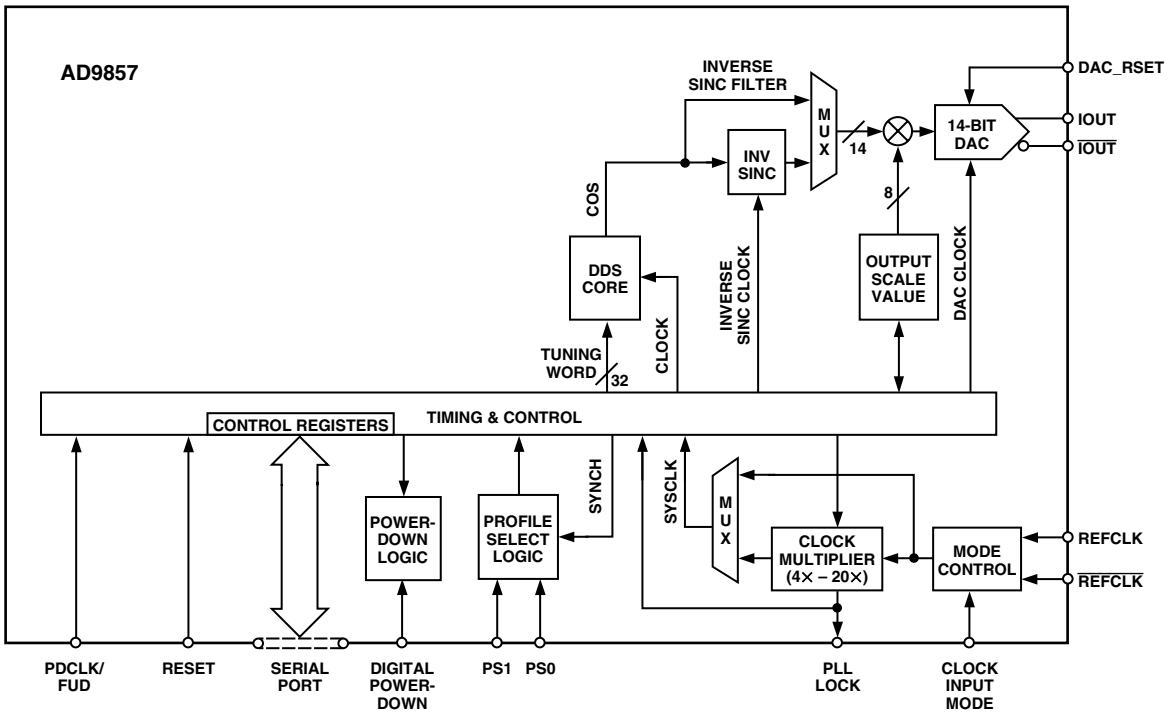


Figure 17. Single-Tone Mode

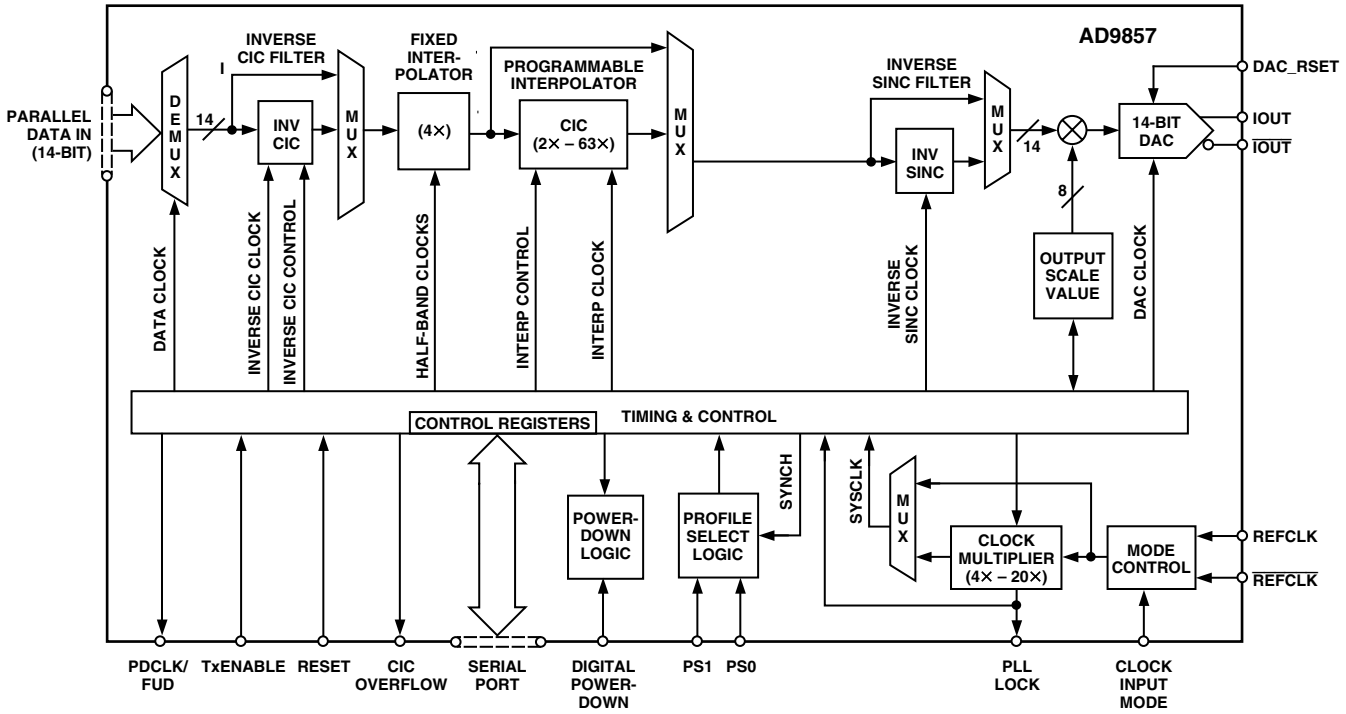


Figure 18. Interpolating DAC Mode

Interpolating DAC Mode

A block diagram of the AD9857 operating in the Interpolating DAC Mode is shown in Figure 18. In this mode the DDS and modulator are both disabled and only the I data path is active. The Q data path is disabled from the 14-bit Parallel Data Port up to and including the modulator.

As with the Quadrature Modulation Mode, the PDCLK pin is an output and functions as a clock which serves to synchronize the input of data to the AD9857. Unlike the Quadrature Modulation Mode, however, the PDCLK operates at the rate of the I data path. This is because only I data is being presented to the parallel port as opposed to the interleaved I/Q format of the Quadrature Modulation Mode.

In the Interpolating DAC Mode, the baseband data supplied at the parallel port remains at baseband at the output; i.e., no modulation takes place. However, a sample rate conversion takes place based on the programmed interpolation rate. The interpolation hardware performs the necessary signal processing required to eliminate the aliased images at baseband that would otherwise result from a sample rate conversion. The interpolating DAC function is effectively an oversampling operation with the original input spectrum intact but sampled at a higher rate.

Signal Processing Path

To better understand the operation of the AD9857 it is helpful to follow the signal path from input, through the device, to the output, examining the function of each block (refer to the Functional Block Diagram). The input to the AD9857 is a 14-bit parallel data path. This assumes that the user is supplying the data as interleaved I and Q values. Any encoding, interpolation, and pulse shaping of the data stream should occur *before* the data is presented to the AD9857 for upsampling.

The AD9857 demultiplexes the interleaved I and Q data into two separate data paths inside the part. This means that the input sample rate (f_{DATA}), the rate at which 14-bit words are presented to the AD9857, must be 2× the internal I/Q Sample Rate (f_{IQ}), the rate at which the I/Q pairs are processed. In other words, $f_{DATA} = 2 \times f_{IQ}$.

From the input demultiplexer to the Quadrature Modulator, the data path of the AD9857 is a dual I/Q path.

All timing within the AD9857 is provided by the internal System Clock (SYSCLK) signal. The externally provided Reference Clock signal may be used as is (1×), or multiplied by the internal Clock Multiplier (4×–20×) to generate the SYSCLK. All other internal clocks and timing are derived from the SYSCLK.

Input Data Assembler

In the Quadrature Modulation or Interpolating DAC Modes the device accepts 14-bit, two's complement data at its parallel data port. The timing of the data supplied to the parallel port may be easily facilitated with the PDCLK/FUD pin of the AD9857, which is an output in the Quadrature Modulation Mode and the Interpolating DAC mode. In the Single-Tone Mode, the same pin becomes an input to the device and serves as a FREQUENCY UPDATE (FUD) strobe.

Frequency control words are programmed into the AD9857 via the serial port (see the Control Register Description). Since the serial port is an asynchronous interface, when programming new frequency tuning words into the on-chip profile registers, the AD9857's internal frequency synthesizer must be synchronized with external events. The purpose of the FUD input pin is to synchronize the start of the frequency synthesizer to the external timing requirements of the user. The rising edge of the FUD signal causes the frequency tuning word of the selected profile

(see the Profile section) to be transferred to the accumulator of the DDS, thus starting the frequency synthesis process.

After loading the frequency tuning word to a profile, a FUD signal is not needed when switching between profiles using the two profile select pins (PS0, PS1). When switching between profiles, the frequency tuning word in the profile register is becomes effective.

In the Quadrature Modulation mode the PDCLK rate is *twice* the rate of the I (or Q) data rate. The AD9857 expects interleaved I and Q data words at the parallel port with one word per PDCLK rising edge. One I word and one Q word together comprise one internal *sample*. Each sample is propagated along the internal data pathway in parallel.

In the Interpolating DAC mode, however, the PDCLK rate is the same as the "I" data rate since the "Q" data path is inactive. In this mode, each PDCLK rising edge latches a data word into the "I" data path.

The PDCLK is provided as a continuous clock (i.e., always active). However, the assertion of PDCLK may be optionally qualified internally by the PLL Lock Indicator if the user elects to set the PLL Lock Control bit in the appropriate Control Register.

Data supplied by the user to the 14-bit Parallel Port is latched into the device coincident with the rising edge of the PDCLK.

In the Quadrature Modulation Mode the rising edge of the TxENABLE signal is used to synchronize the device. While TxENABLE is in the Logic 0 state, the device ignores the 14-bit data applied to the parallel port and allows the internal data path to be flushed by forcing 0s down the I and Q data pathway. On the rising edge of TxENABLE the device is ready for the first "I" word. The first "I" word is latched into the device coincident with the rising edge of PDCLK. The next rising edge of PDCLK latches in a "Q" word, etc., until TxENABLE is set to a Logic 0 state by the user.

When in the Quadrature Modulation Mode it is important that the user ensure that an even number of PDCLK intervals are observed during any given TxENABLE period. This is because the device must capture *both* an I and a Q value before the data can be processed along the internal data pathway.

The timing relationship between TxENABLE, PDCLK, and DATA is shown in Figures 19 and 20.

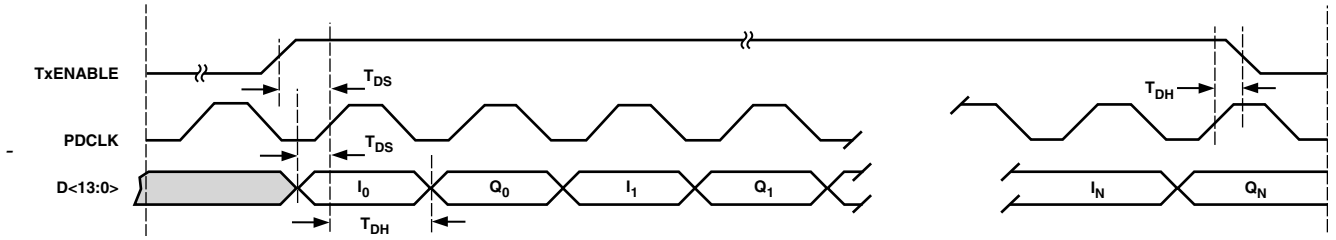


Figure 19. 14-Bit Parallel Port Timing Diagram—Quadrature Modulation Mode

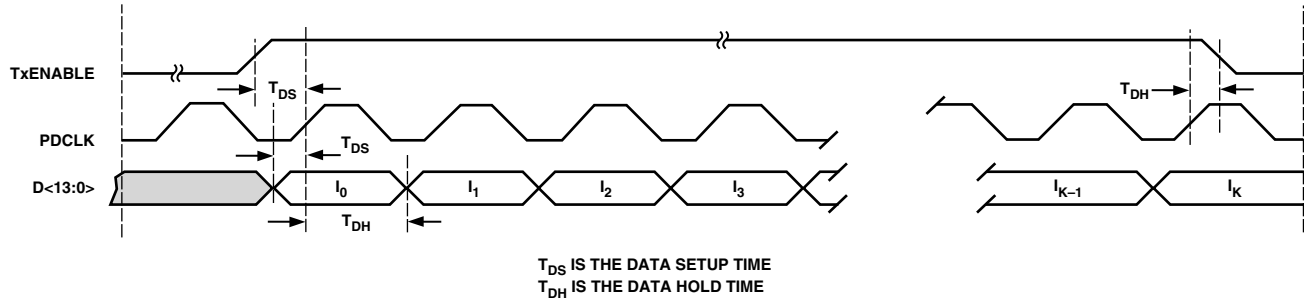


Figure 20. 14-Bit Parallel Port Timing Diagram—Interpolating DAC Mode

Inverse CIC Filter

The Inverse CIC Filter precompensates the data in order to offset the slight attenuation gradient imposed by the CIC filter (see the Programmable (2×–63×) CIC Interpolating Filter section). The I (or Q) data entering the first half-band filter occupies a maximum bandwidth of one-half f_{DATA} as defined by Nyquist (where f_{DATA} is the sample rate at the input of the first half-band filter). This is shown graphically in Figure 21.

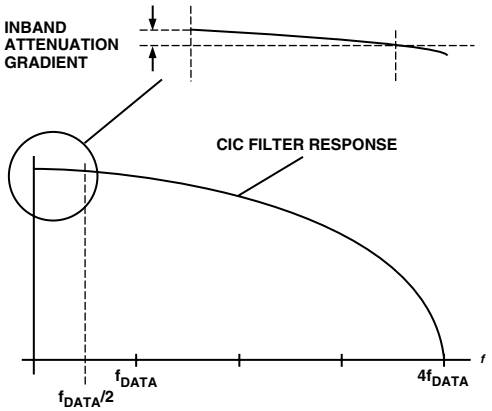


Figure 21. CIC Filter Response

Table I. Parallel Data Bus Timing

Symbol	Definition	Min
t_{DS}	Data Setup Time	4 ns
t_{DH}	Data Hold Time	0 ns

If the CIC filter is employed, the inband attenuation gradient could pose a problem for those applications requiring an extremely flat pass band. For example, if the spectrum of the data as supplied to the AD9857 I or Q path occupies a significant portion of the one-half f_{DATA} region, the higher frequencies of the data spectrum will receive slightly more attenuation than the lower frequencies (the worst-case overall droop from f = 0 to one-half f_{DATA} is < 0.8 dB). This may not be acceptable in certain applications. The Inverse CIC filter has a response characteristic that is the inverse of the CIC filter response over the one-half f_{DATA} region.

The net result is that the product of the two responses yields in an extremely flat pass band, thereby eliminating the inband attenuation gradient introduced by the CIC filter. The price to be paid is a slight attenuation of the input signal of approximately 0.5 dB for a CIC interpolation rate of 2 dB and 0.8 dB for interpolation rates of 3 to 63.

The Inverse CIC Filter is implemented as a digital FIR filter with a response characteristic that is the inverse of the Programmable CIC Interpolator. The product of the two responses yields a nearly flat response over the baseband Nyquist bandwidth. The Inverse CIC filter provides frequency compensation that yields a response flatness of ±0.05 dB over the baseband Nyquist bandwidth, allowing the AD9857 to provide excellent SNR over its performance range.

The Inverse CIC Filter can be bypassed by setting Control Register 06h<0>. It is automatically bypassed if the CIC interpolation rate is 1×. Whenever this stage is bypassed, power to the stage is shut off, thereby reducing power dissipation.

Fixed Interpolator (4×)

This block is a fixed 4× interpolator. It is implemented as two half-band filters. The output of this stage is the original data upsampled by 4×.

Before presenting a detailed description of the half-band filters, recall that in the case of the Quadrature Modulation Mode the input data stream is representative of complex data; i.e., two input samples are required to produce one I/Q data pair. The I/Q sample rate is one-half the input data rate. The I/Q sample rate (the rate at which I or Q samples are presented to the input of the first half-band filter) will be referred to as f_{IQ}. Since the AD9857 is a quadrature modulator, f_{IQ} represents the baseband of the internal I/Q sample pairs. It should be emphasized here that f_{IQ} is not the same as the baseband of the user's symbol rate data, which must be upsampled before presentation to the AD9857 (as will be explained later). The I/Q sample rate (f_{IQ}) puts a limit on the minimum bandwidth necessary to transmit the f_{IQ} spectrum. This is the familiar Nyquist limit and is equal to one-half f_{IQ}, hereafter referred to as f_{NYQ}.

Together, the two half-band filters provide a factor-of-four increase in the sampling rate ($4 \times f_{IQ}$ or $8 \times f_{NYQ}$). Their combined insertion loss is 0.01 dB, so virtually no loss of signal level occurs through the two half-band filters. Both half-band filters are linear phase filters, so that virtually no phase distortion is introduced within the pass band of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

The half-band filters are designed so that their composite performance yields a usable pass band of 80% of the baseband Nyquist frequency (0.2 on the frequency scale below). Within that pass band the ripple will not exceed 0.002 dB. The stopband extends from 120% to 400% of the baseband Nyquist frequency (0.3 to 1.0 on the frequency scale below) and offers a minimum of 85 dB attenuation. The composite response of the two half-band filters together are shown in Figures 22 and 23.

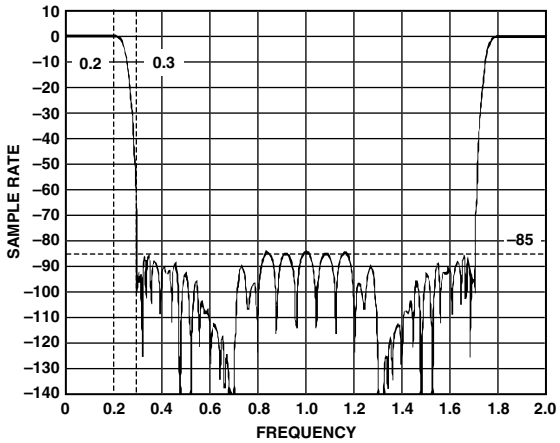


Figure 22. Half-Band 1 and 2 Frequency Response; Frequency Relative to HB1 Output Sample Rate

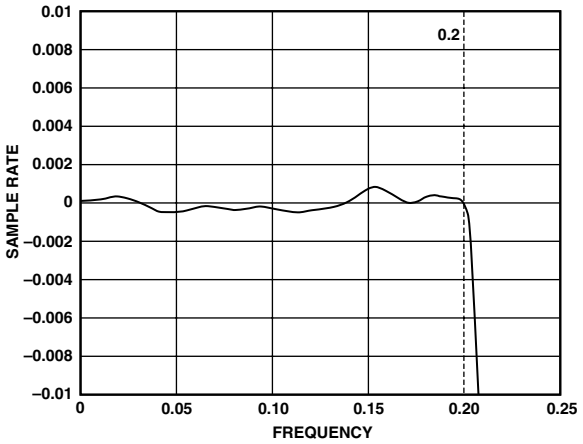


Figure 23. Half-Band 1 and 2 Pass Band Detail; Frequency Relative to HB1 Output Sample Rate

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9857. A look at the pass band detail of the half-band filter response indicates that in order to maintain an amplitude error of no more than 1 dB, we are restricted to signals having a bandwidth of no more than about 90% of f_{NYQ}. Thus, in order to keep the bandwidth of the data in the flat portion of the filter pass band, the user must oversample the baseband data by at least a factor of two prior to presenting it to the AD9857. Note that without oversampling, the Nyquist bandwidth of the baseband data corresponds to the f_{NYQ}. Because of this, the upper end of the data bandwidth will suffer 6 dB or more of attenuation due to the frequency response of the half-band filters. Furthermore, if the baseband data applied to the AD9857 has been pulse shaped there is an additional concern.

Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that $0 \leq \alpha \leq 1$. A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and $\alpha = 1$, the Nyquist bandwidth of the data will correspond with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the roll-off attenuation of the half-band filters. The following diagrams illustrate the relationship between α and the bandwidth of raised cosine shaped pulses. The problem area is indicated by the shading in the tail of the pulse with $\alpha = 1$, which extends into the roll-off region of the half-band filter.

The effect of raised cosine filtering on baseband pulse bandwidth, and the relationship to the half-band filter response is shown in Figure 24.

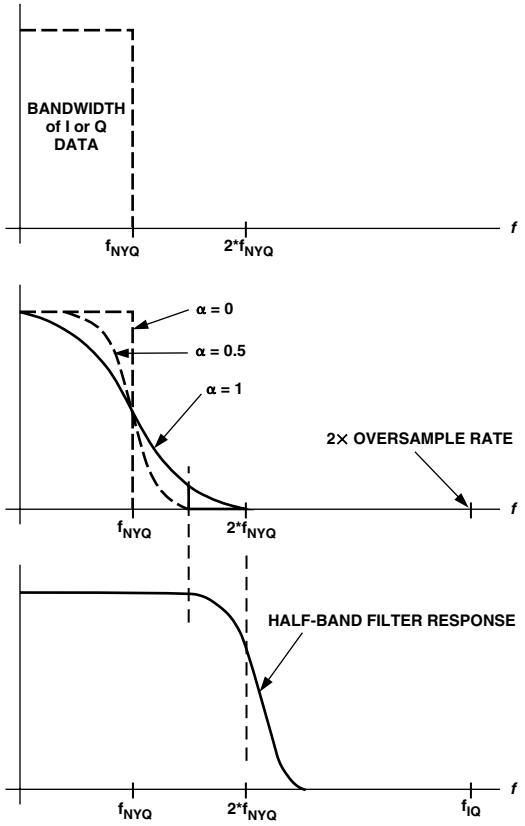


Figure 24. Effect of Alpha

Programmable (2×–63×) CIC Interpolating Filter

The Programmable Interpolator is implemented as a CIC (Cascaded Integrator-Comb) filter. It is programmable by a 6-bit control word, giving a range of 2× to 63× interpolation. This interpolator has a low-pass frequency characteristic that is compensated by the Inverse CIC filter.

The Programmable Interpolator can be bypassed to yield a 1× (no interpolation) configuration by setting the bit in the appropriate control register, per each profile. Whenever the Programmable Interpolator is bypassed (1× CIC rate) power to the stage is removed. If the Programmable Interpolator is bypassed, the Inverse CIC filter (see above) is automatically bypassed, since its compensation is not needed in this case.

The output of the Programmable Interpolator is the data from the 4× interpolator upsampled by an additional 2× to 63×, according to the rate chosen by the user. This results in the input data being upsampled by a factor of 8× to 252×.

The transfer function of the CIC Interpolating Filter is:

$$H(f) = \left(\sum_{k=0}^{R-1} e^{-j(2 \times \pi \times f \times k} \right)^5$$

where R is the interpolation rate, and f is the frequency relative to SYSCLK.

Quadrature Modulator

The digital quadrature modulator stage is used to frequency shift the *baseband* spectrum of the incoming data stream up to the desired carrier frequency (this process is known as *upconversion*).

It should be noted that at this point the incoming data has been converted from an incoming sampling rate of f_{IN} to an I/Q sampling rate equal to SYSCLK. The purpose of the upsampling process is to make the data sampling rate equal to the sampling rate of the carrier signal.

The carrier frequency is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS uses the internal reference clock (SYSCLK) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that represents the *quadrature modulated carrier.*

A key point is that the modulation is done digitally which eliminates the phase and gain imbalance and crosstalk issues typically associated with analog modulators. Note that the modulated "signal" is actually a number stream sampled at the rate of SYSCLK, the same rate at which the output D/A converter is clocked.

The quadrature modulator operation is also controlled by spectral invert bits in each of the four profiles. The quadrature modulation takes the form:

$I \times COS(\omega) + Q \times SIN(\omega)$ when the spectral invert bit is set to a Logic 1.

$I \times COS(\omega) - Q \times SIN(\omega)$ when the spectral invert bit is set to a Logic 0.

DDS Core

The direct digital synthesizer (DDS) block generates the sin/cos carrier reference signals that digitally modulate the I/Q data paths. The DDS frequency is tuned via the serial control port with a 32-bit tuning word (per profile). This allows the AD9857's output carrier frequency to be very precisely tuned while still providing output frequency agility.

The equation relating output frequency (f_{OUT}) of the AD9857 digital modulator to the frequency tuning word (FTWORD) and the system clock (SYSCLK) is:

$$f_{OUT} = (FTWORD \times SYSCLK)/2^{32}$$

where f_{OUT} and *SYSCLK* frequencies are in Hz and *FTWORD* is a decimal number from 0 to 2,147,483,647 (2^{31}–1)

Example: Find the FTWORD for f_{OUT} = 41 MHz and SYSCLK = 122.88 MHz

If f_{OUT} = 41 MHz and SYSCLK = 122.88 MHz, then

$$FTWORD = 556AAAAB\ hex$$

Loading 556AAAABh into control bus registers 08h–0Bh (for Profile 1) programs the AD9857 for f_{OUT} = 41 MHz, given a SYSCLK frequency of 122.88 MHz.

Inverse SINC Filter

The sampled carrier data stream is the input to the digital-to-analog converter (DAC) integrated onto the AD9857. The DAC output spectrum is shaped by the characteristic sin(x)/x (or SINC) envelope, due to the intrinsic zero-order hold effect associated with DAC-generated signals. Since the shape of the SINC envelope is well known, it can be compensated for. This envelope restoration function is provided by the optional inverse SINC filter preceding the DAC. This function is implemented as an FIR filter, which has a transfer function that is the exact inverse of the SINC response. When the Inverse SINC Filter is selected, it modifies the incoming data stream so that the desired carrier envelope, which would otherwise be shaped by the SINC envelope, is restored. It should be noted, however, that this correction is only complete for carrier frequencies up to approximately 45% of SYSCLK.

It should be noted that the inverse SINC filter introduces about a 3.5 dB loss at low frequencies as compared to the gain with the inverse SINC filter turned off. This is done to flatten the overall gain from dc to 45% of SYSCLK.

The inverse SINC filter can be bypassed if it is not needed. If the inverse SINC filter is bypassed, its clock is stopped, thus reducing the power dissipation of the part.

Output Scale Multiplier

An 8-bit multiplier (*Output Scale Value* in the block diagram) preceding the DAC provides the user with a means of adjusting the final output level. The multiplier value is programmed via the appropriate control registers, per each profile. The LSB weight is 2^{-7}, which yields a multiplier range of 0 to 1.9921875, or nearly 2×. Since the quadrature modulator has an intrinsic loss of 3 dB ($1/\sqrt{2}$), programming the multiplier for a value of $\sqrt{2}$) will restore the data to the full-scale range of the DAC when the device is operating in the Quadrature Modulation Mode. Since the AD9857 defaults to the Modulation Mode, the default value for the multiplier is B5h (which corresponds to $\sqrt{2}$).

Programming the output scale multiplier to unity gain (80h) bypasses the stage, reducing power dissipation.

14-Bit D/A Converter

A 14-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst-case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (please see Analog Devices, *DDS Tutorial* at **http://www.analog.com/dds** for a detailed explanation of aliases). The wideband 14-bit DAC in the AD9857 maintains spurious-free dynamic range (SFDR) performance of –60 dBc up to A_{OUT} = 42 MHz and –55 dBc up to A_{OUT} = 65 MHz.

The conversion process will produce aliased components of the fundamental signal at n × SYSCLK ± FCARRIER (n = 1, 2, 3). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest to avoid modulation impairments.

The AD9857 provides true and complemented current outputs on A_{OUT} and $\overline{A_{OUT}}$ respectively. The full-scale output current is set by the RSET resistor at DAC_RSET. The value of RSET for a particular IOUT is determined using the following equation:

$$RSET = 39.93/IOUT$$

For example, if a full-scale output current of 20 mA is desired, then *RSET* = (39.93/0.02), or approximately 2 kΩ. Every doubling of the RSET value will halve the output current.

The full-scale output current range of the AD9857 is 5 mA–20 mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching; the two outputs should be terminated equally for best SFDR performance.

The output load should be located as close as possible to the AD9857 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit.

Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance. Therefore, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9857 will see for signals within the filter pass band. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9857.

The output compliance voltage of the AD9857 is –0.5 V to +1.0 V. Any signal developed at the DAC output should not exceed 1.0 V, otherwise, signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The use of a transformer with a grounded center-tap for common-mode rejection results in signals at the AD9857 DAC output pins that are symmetrical about ground.

As previously mentioned, by differentially combining the two signals the user can provide some degree of common-mode signal rejection. A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or "clock feed-through" that is equally present on both input signals. The AD9857 true and complement outputs can be differentially combined using a broadband 1:1 transformer with a grounded, center-tapped primary to perform differential combining of the two DAC outputs.

Reference Clock Multiplier

It is often difficult to provide a high-quality oscillator with an output in the frequency range of 100 MHz–200 MHz. The AD9857 allows the use of a lower-frequency oscillator that can be multiplied to a higher frequency by the on-board Reference Clock Multiplier, implemented with a Phase Locked Loop architecture. See the Ease of Use section for a more thorough discussion of the Reference Clock Multiplier feature.

INPUT DATA PROGRAMMING

Control Interface—Serial I/O

The AD9857 serial port is a flexible, synchronous, serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9857. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9857's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

General Operation of the Serial Interface

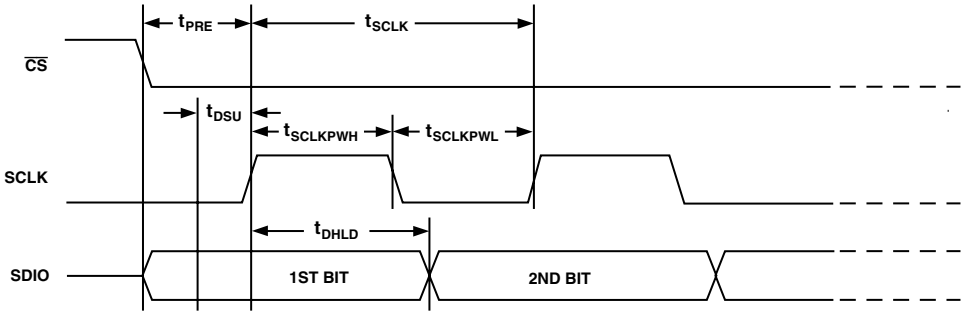
There are two phases to a communication cycle with the AD9857. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9857, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9857 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer (1–4), and the starting register address for the first byte of the data transfer.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9857. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9857 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one communication cycle in a multibyte transfer is the preferred method. However, single byte communication cycles are useful to reduce CPU overhead when register access requires one byte only. An example of this may be to write the AD9857 SLEEP bit.

At the completion of any communication cycle, the AD9857 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

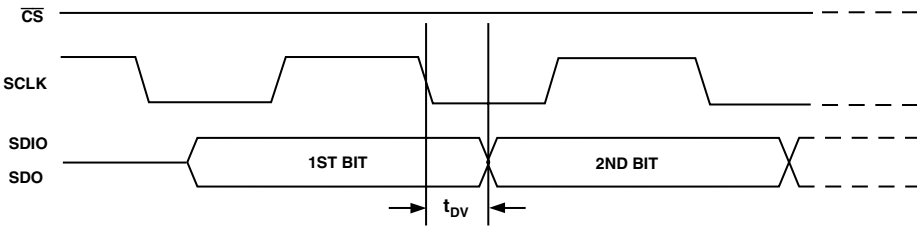
All data input to the AD9857 is registered on the rising edge of SCLK. All data is driven out of the AD9857 on the falling edge of SCLK.

Figures 25 and 26 illustrate the Data Write and Data Read operations on the AD9857 serial port:



SYMBOL	DEFINITION	MIN
t_{PRE}	$\overline{CS}$ SETUP TIME	40ns
t_{SCLK}	PERIOD OF SERIAL DATA CLOCK	100ns
t_{DSU}	SERIAL DATA SETUP TIME	30ns
$t_{SCLKPWH}$	SERIAL DATA CLOCK PULSEWIDTH HIGH	40ns
$t_{SCLKPWL}$	SERIAL DATA CLOCK PULSEWIDTH LOW	40ns
t_{DHLD}	SERIAL DATA HOLD TIME	0ns

Figure 25. Timing Diagram for Data Write to AD9857



SYMBOL	DEFINITION	MAX
t_{DV}	DATA VALID TIME	30ns

Figure 26. Timing Diagram for Read from AD9857

Figures 27–30 are useful in understanding the general operation of the AD9857 Serial Port.

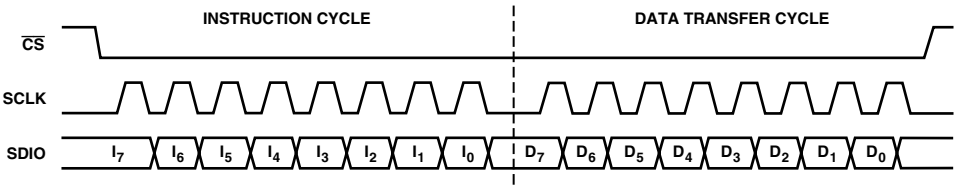


Figure 27. Serial Port Writing Timing—Clock Stall Low

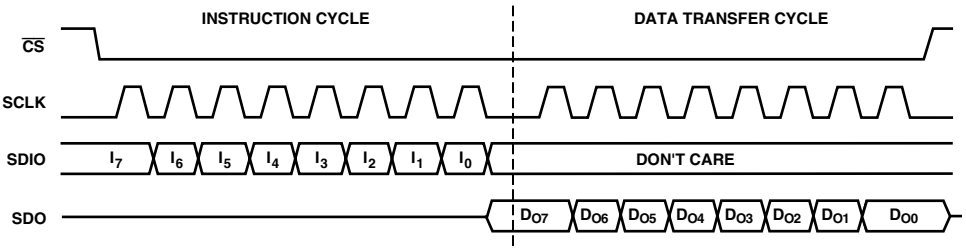


Figure 28. 3-Wire Serial Port Read Timing—Clock Stall Low

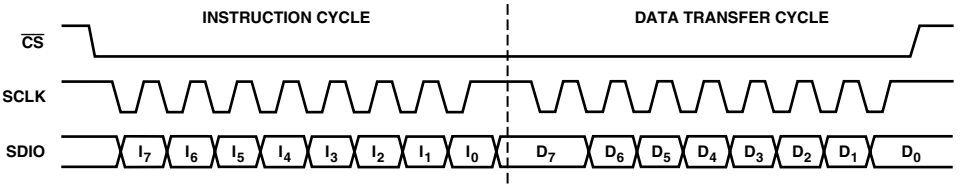


Figure 29. Serial Port Write Timing—Clock Stall High

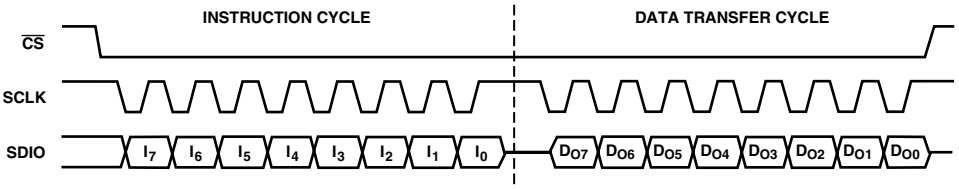


Figure 30. 2-Wire Serial Port Read Timing—Clock Stall High

Instruction Byte

The instruction byte contains the following information as shown in Table II.

Table II. Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$—Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

N1, N0—Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle of the communications cycle. The bit decodes are shown in Table III.

Table III. N1, N2 Decode Bits

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9857.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9857 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

$\overline{CS}$—Chip Select. Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high-impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO—Serial Data I/O. Data is always written into the AD9857 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 00h. The default is logic zero, which configures the SDIO pin as bidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9857 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high-impedance state.

SYNCIO—Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the SYNC I/O pin causes the current communication cycle to abort. After SYNC I/O returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

MSB/LSB Transfers

The AD9857 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the Control Register 00h<6> bit. The default value of Control Register 00h<6> is low (MSB first). When Control Register 00h<6> is set high, the AD9857 serial port is in LSB first format. The instruction byte must be written in the format indicated by Control Register 00h<6>. That is, if the AD9857 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

Notes on Serial Port Operation

The AD9857 serial port configuration bits reside in Bits 6 and 7 of register address 0h. It is important to note that the configuration changes immediately upon writing to this register. For multibyte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

The AD9857 serial port controller address will roll from 19h to 0h for multibyte I/O operations if the MSB first mode is active. The serial port controller address will roll from 0h to 19h for multibyte I/O operations if the LSB first mode is active.

The system must maintain synchronization with the AD9857 or the internal control logic will not be able to recognize further instructions. For example, if the system sends an instruction byte for a 2-byte write, then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9857, but the next eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9857, the SYNC I/O pin provides a means to re-establish synchronization without reinitializing the entire chip. The SYNC I/O pin enables the user to reset the AD9857 state machine to accept the next eight SCLK rising edges to be coincident with the instruction phase of a new communication cycle. By applying and removing a “high” signal to the SYNC I/O pin, the AD9857 is set to once again begin performing the communication cycle in synchronization with the system. Any information that had been written to the AD9857 registers during a valid communication cycle prior to loss of synchronization will remain intact.

CONTROL REGISTER DESCRIPTION

Reference Clock (REFCLK) Multiplier—Register Address 00h, Bits 0, 1, 2, 3, 4

A 5-bit number (M), the value of which determines the multiplication factor for the internal PLL (Bit 4 is the MSB). The system clock (SYSCLK) is M times the frequency of the REFCLK input signal. If M = 01h, the PLL circuit is bypassed and $f_{SYSCLK} = f_{REFCLK}$. If 04h ≤ M ≤ 14h, the PLL multiplies the REFCLK frequency by M (4–20 decimal). Any other value of M is considered an invalid entry.

PLL Lock Control—Register Address 00h, Bit 5

When set to a logic 0, the device uses the status of the PLL Lock Indicator pin to internally control the operation of the 14-bit parallel data path. When set to a Logic 1, the internal control logic ignores the status of the PLL Lock Indicator pin.

LSB First—Register Address 00h, Bit 6

When set to a Logic 1, the serial interface accepts serial data in LSB First format. When set to a Logic 0, MSB First format is assumed.

SDIO Input Only—Register Address 00h, Bit 7

When set to a Logic 1, the serial data I/O pin (SDIO) is configured as an input only pin. When set to a logic 0, the SDIO pin has bidirectional operation.

Operating Mode—Register Address 01h, Bits 0, 1

00h: Selects the Quadrature Modulation Mode of operation.
01h: Selects the Single-Tone Mode of operation.
02h: Selects the Interpolating DAC Mode of operation.
03h: Invalid entry.

Auto Power-Down—Register Address 01h, Bit 2

When set to a Logic 1, the device automatically switches into its low-power mode whenever TxENABLE is deasserted for a sufficiently long period of time. When set to a Logic 0, the device only powers down in response to the Digital Power-Down pin.

Full Sleep Mode—Register Address 01h, Bit 3

When set to a Logic 1, the device completely shuts down.

Reserved—Register Address 01h, Bit 4

Reserved—Register Address 01h, Bit 5

This bit must always be set to 0.

Inverse SINC Bypass—Register Address 01h, Bit 6

When set to a Logic 1, the Inverse Sinc filter is BYPASSED. When set to a Logic 0, the Inverse Sinc filter is active.

CIC Clear—Register Address 01h, Bit 7

When set to a Logic 1, the CIC filters are cleared. When set to a Logic 0, the CIC filters operate normally.

PROFILE #0

Tuning Word—Register Address 02h, Bits 0, 1, 2, 3, 4, 5, 6, 7

The lower byte of the 32-bit frequency tuning word, Bits 0–7.

Tuning Word—Register Address 03h, Bits 0, 1, 2, 3, 4, 5, 6, 7

The second byte of the 32-bit frequency tuning word, Bits 8–15.

Tuning Word—Register Address 04h, Bits 0,1, 2, 3, 4, 5, 6, 7

The third byte of the 32-bit frequency tuning word, Bits 16–23.

Tuning Word—Register Address 05h, Bits 0, 1, 2, 3, 4, 5, 6, 7

The fourth byte of the 32-bit frequency tuning word, Bits 24–31.

Inverse CIC Bypass—Register Address 06h, Bit 0

When set to a Logic 1, the Inverse CIC filter is BYPASSED. When set to a Logic 0, the Inverse CIC filter is active.

Spectral Invert—Register Address 06h, Bit 1

The quadrature modulator takes the form:

$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 1.
$I \times \cos(\omega) - Q \times \sin(\omega)$ when set to a Logic 0.

CIC Interpolation Rate—Register Address 06h, Bits 2, 3, 4, 5, 6, 7

00h: Invalid entry.
01h: CIC filters BYPASSED.
02h–3Fh: CIC interpolation rate (2–63, decimal).

Output Scale Factor—Register Address 07h, Bits 0, 1, 2, 3, 4, 5, 6, 7

An 8-bit number that serves as a multiplier for the data pathway before the data is delivered the DAC. It has an LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

PROFILE #1

Tuning Word—Register Address 08h, Bits 0, 1, 2, 3, 4, 5, 6, 7

The lower byte of the 32-bit frequency tuning word, Bits 0–7.

Tuning Word—Register Address 09h, Bits 0, 1, 2, 3, 4, 5, 6, 7

The second byte of the 32-bit frequency tuning word, Bits 8–15.

Tuning Word—Register Address 0Ah, Bits 0, 1, 2, 3, 4, 5, 6, 7

The third byte of the 32-bit frequency tuning word, Bits 16–23.

Tuning Word—Register Address 0Bh, Bits 0, 1, 2, 3, 4, 5, 6, 7

The fourth byte of the 32-bit frequency tuning word, Bits 24–31.

Inverse CIC Bypass—Register Address 0Ch, Bit 0

When set to a Logic 1, the Inverse CIC filter is BYPASSED. When set to a Logic 0, the Inverse CIC filter is active.

Spectral Invert—Register Address 0Ch, Bit 1

The quadrature modulator takes the form:

$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 1.
$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 0.

CIC Interpolation Rate—Register Address 0Ch, Bits 2, 3, 4, 5, 6, 7

00h: Invalid entry.
01h: CIC filters BYPASSED.
02h–3Fh: CIC interpolation rate (2–63, decimal).

Output Scale Factor—Register Address 0Dh, Bits 0, 1, 2, 3, 4, 5, 6, 7

An 8-bit number that serves as a multiplier for the data pathway before the data is delivered the DAC. It has an LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

PROFILE #2

Tuning Word—Register Address 0Eh, Bits 0, 1, 2, 3, 4, 5, 6, 7
The lower byte of the 32-bit frequency tuning word, Bits 0–7.

Tuning Word—Register Address 0Fh, Bits 0, 1, 2, 3, 4, 5, 6, 7
The second byte of the 32-bit frequency tuning word, Bits 8–15.

Tuning Word—Register Address 10h, Bits 0, 1, 2, 3, 4, 5, 6, 7
The third byte of the 32-bit frequency tuning word, Bits 16–23.

Tuning Word—Register Address 11h, Bits 0, 1, 2, 3, 4, 5, 6,7
The fourth byte of the 32-bit frequency tuning word, Bits 24–31.

Inverse CIC Bypass—Register Address 12h, Bit 0
When set to a Logic 1, the Inverse CIC filter is BYPASSED.
When set to a Logic 0, the Inverse CIC filter is active.

Spectral Invert—Register Address 12h, Bit 1
The quadrature modulator takes the form:
$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 1.
$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 0.

CIC Interpolation Rate—Register Address 12h, Bits 2, 3, 4, 5, 6, 7
00h: Invalid entry.
01h: CIC filters BYPASSED.
02h–3Fh: CIC interpolation rate (2–63, decimal).

Output Scale Factor—Register Address 13h, Bits 0, 1, 2, 3, 4, 5, 6, 7
An 8-bit number that serves as a multiplier for the data pathway before the data is delivered the DAC. It has an LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

PROFILE #3

Tuning Word—Register Address 14h, Bits 0, 1, 2, 3, 4, 5, 6, 7
The lower byte of the 32-bit frequency tuning word, Bits 0–7.

Tuning Word—Register Address 15h, Bits 0, 1, 2, 3, 4, 5, 6, 7
The second byte of the 32-bit frequency tuning word, Bits 8–15.

Tuning Word—Register Address 16h, Bits 0, 1, 2, 3, 4, 5, 6, 7
The third byte of the 32-bit frequency tuning word, Bits 16–23.

Tuning Word—Register Address 17h, Bits 0, 1, 2, 3, 4, 5, 6, 7
The fourth byte of the 32-bit frequency tuning word, Bits 24–31.

Inverse CIC Bypass—Register Address 18h, Bit 0
When set to a Logic 1, the Inverse CIC filter is BYPASSED.
When set to a Logic 0, the Inverse CIC filter is active.

Spectral Invert—Register Address 18h, Bit 1
The quadrature modulator takes the form:
$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 1.
$I \times \cos(\omega) + Q \times \sin(\omega)$ when set to a Logic 0.

CIC Interpolation Rate—Register Address 18h, Bits 2, 3, 4, 5, 6, 7
00h: Invalid entry.
01h: CIC filters BYPASSED.
02h–3Fh: CIC interpolation rate (2–63, decimal).

Output Scale Factor—Register Address 19h, Bits 0, 1, 2, 3, 4, 5, 6, 7
An 8-bit number that serves as a multiplier for the data pathway before the data is delivered the DAC. It has an LSB weight of 2^{-7} (0.0078125). This yields a multiplier range of 0 to 1.9921875.

Table IV. Control Register Quick Reference

Reg Addr	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value	Profile
00h	SDIO Input Only	LSB First	PLL Lock Control	**REFCLK Multiplier** 01h: *Bypass* PLL 04h–14h: 4×–20×					21h	N/A
01h	CIC Clear	Inverse SINC Bypass	Reserved: Must Be 0	Reserved	Full Sleep	Auto Power-Down	**Operating Mode** 00h: Quad. Mod. 01h: Single-Tone 02h: Intrp. DAC		00h	N/A
02h	Frequency Tuning Word #1 <7:0>								00h	0
03h	Frequency Tuning Word #1 <15:8>								00h	0
04h	Frequency Tuning Word #1 <23:16>								00h	0
05h	Frequency Tuning Word #1 <31:24>								00h	0
06h	**CIC Interpolation Rate** 01h: Bypass CIC Filter 02h–3Fh: Interpolation Factor (2–63, Decimal)						Spectral Invert	Inverse CIC Bypass	08h	0
07h	**Output Scale Factor** Bit Weighting: MSB = 2^0, LSB = 2^{-7}								B5h	0
08h	Frequency Tuning Word #2 <7:0>								Unset	1
09h	Frequency Tuning Word #2 <15:8>								Unset	1
0Ah	Frequency Tuning Word #2 <23:16>								Unset	1
0Bh	Frequency Tuning Word #2 <31:24>								Unset	1
0Ch	**CIC Interpolation Rate** 01h: Bypass CIC Filter 02h–3Fh: Interpolation Factor (2–63, Decimal)						Spectral Invert	Inverse CID Bypass	Unset	1
0Dh	**Output Scale Factor** Bit Weighting: MSB = 2^0, LSB = 2^{-7}								Unset	1
0Eh	Frequency Tuning Word #3 <7:0>								Unset	2
0Fh	Frequency Tuning Word #3 <15:8>								Unset	2
10h	Frequency Tuning Word #3 <23:16>								Unset	2
11h	Frequency Tuning Word #3 <31:24>								Unset	2
12h	**CIC Interpolation Rate** 01h: Bypass CIC Filter 02h–3Fh: Interpolation Factor (2–63, Decimal)						Spectral Invert	Inverse CIC Bypass	Unset	2
13h	**Output Scale Factor** Bit Weighting: MSB = 2^0, LSB = 2^{-7}								Unset	2
14h	Frequency Tuning Word #4 <7:0>								Unset	3
15h	Frequency Tuning Word #4 <15:8>								Unset	3
16h	Frequency Tuning Word #4 <23:16>								Unset	3
17h	Frequency Tuning Word #4 <31:24>								Unset	3
18h	**CIC Interpolation Rate** 01h: Bypass CIC Filter 02h–3Fh: Interpolation Factor (2–63, Decimal)						Spectral Invert	Inverse CIC Bypass	Unset	3
19h	**Output Scale Factor** Bit Weighting: MSB = 2^0, LSB = 2^{-7}								Unset	3

Latency

The latency through the AD9857 is easiest to describe in terms of System Clock (SYSCLK) cycles. Latency is a function of the AD9857 configuration (that is, which mode and which optional features are engaged). The latency is primarily affected by the programmable interpolator's rate.

The following values should be considered estimates because observed latency may be data-dependent. The latency was calculated using the linear delay model for FIR filters.

SYSCLK = *REFCLK* × *Reference Clock Multiplier Factor*
(1 *If Bypassed*, 4–20)

N = *Programmable Interpolate Rate*
(1 *If Bypassed*, 2–63)

Table V.

Stage	Modulator Mode	Interpolator Mode
Input Demux	4 × N	8 × N
Inverse CIC	12 × N (Optional)	12 × N (Optional)
Fixed Interpolator	82 × N	82 × N
Programmable Interpolator	5 × N + 9	5 × N + 9
Quadrature Modulator	7	Not Used
Inverse SINC	7 (Optional)	7 (Optional)
Output Scaler	6 (Optional)	6 (Optional)

Example

Interpolate Mode
Clock Multiplier = 4
Inverse CIC = On
Interpolate Rate = 20
Inverse SINC = Off
Output Scale = On

Latency = 8 × 20 + 12 × 20 + 82 × 20 + (5 × 20 + 9) + 6 = 2155 *System Clocks*/4 = 538.75 *Reference Clock Periods*

Latency for the Single-Tone Mode

In Single-Tone Mode, frequency hopping is accomplished by alternately selecting the two profile input pins. The time required to switch from one frequency to another is less than 30 System Clock cycles (SYSCLK) with the Inverse SINC Filter and the Output scaler engaged. With the Inverse SINC Filter disengaged, the latency drops to less than 24 SYSCLK cycles.

Other Factors Affecting Latency

Another factor affecting latency is the internal clock phase relationship at the start of any burst transmission. For systems that need to maintain exact SYSCLK cycle latency for all bursts, the user must be aware of the possible difference in SYSCLK cycle latency through the DEMUX, which precedes the signal processing chain. The timing diagrams of Figures 31 and 32 describe how the latency differs depending upon the phase relationship between the PDCLK and the clock that samples data at the output of the data assembler logic (labeled DEMUX on the block diagram).

Regarding Figures 31 and 32, the SYSCLK/N trace represents the clock frequency that is divided down from SYSCLK by the CIC interpolation rate. That is, with SYSCLK equal 200 MHz and the CIC interpolation rate equal 2 (N = 2), then SYSCLK/N equals 100 MHz. The SYSCLK/2N and SYSCLK/4N signals are divide by 2 and 4 of SYSCLK/N, respectively. For Quadrature Modulation Mode the PDCLK is the SYSCLK/2N frequency and the clock that samples data into the signal processing chain is the SYSCLK/4N frequency. Note that SYSCLK/2N rising edges create the transition of the SYSCLK/4N signal.

Figure 31 shows the timing for a burst transmission that starts when the PDCLK (SYSCLK/2N) signal generates a rising edge on the SYSCLK/4N clock. The latency from the D<13:0> pins to the output of the data assembler logic is three PDCLK cycles. The output is valid on the falling edge of SYSCLK/4N clock and is sampled into the signal processing chain on the next rising edge of the SYSCLK/4N clock (1/2 SYSCLK/4N clock cycle latency).

Figure 32 shows the timing for a burst transmission that starts when the PDCLK (SYSCLK/2N) signal generates a falling edge on the SYSCLK/4N clock. The latency from the D<13:0> pins to the output of the data assembler logic is three PDCLK cycles. This is identical to Figure 31, but note that output is valid on the rising edge of SYSCLK/4N clock and is sampled into the signal processing chain on the next rising edge of the SYSCLK/4N clock (1 full SYSCLK/4N clock cycle latency).

The difference in latency (as related to SYSCLK clock cycles) is SYSCLK/2N, or one PDCLK cycle.

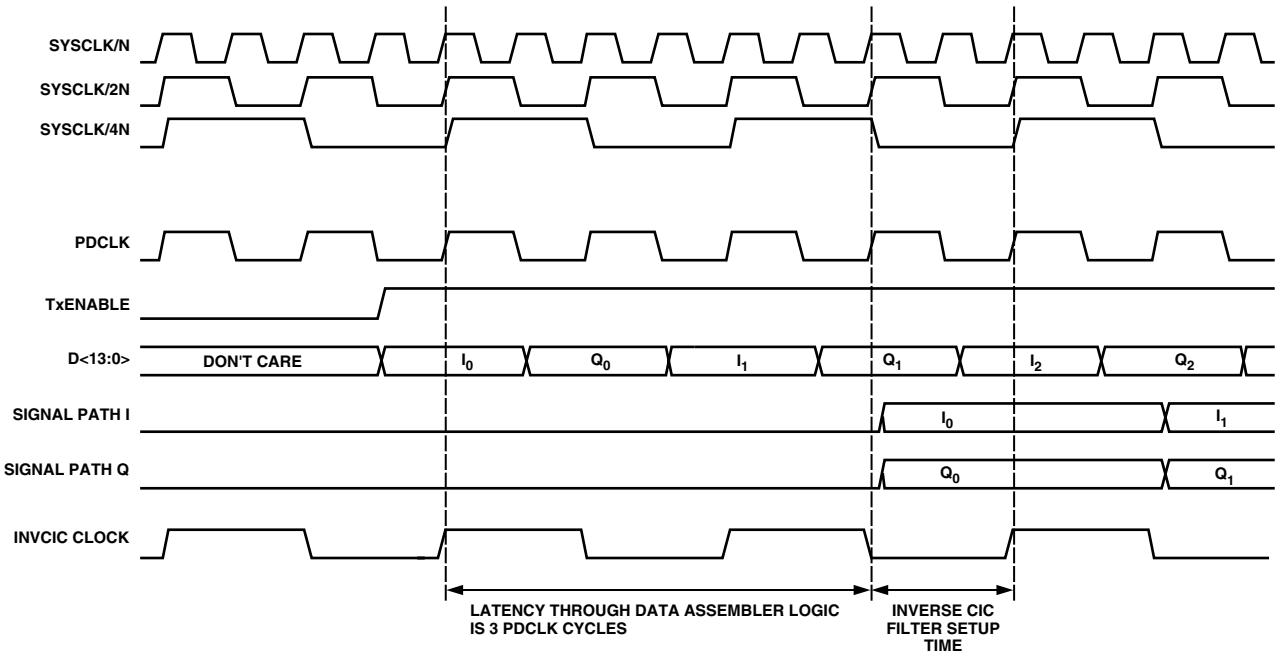


Figure 31. Latency from D<13:0> to Signal Processing Chain, Four PDCLK Cycles

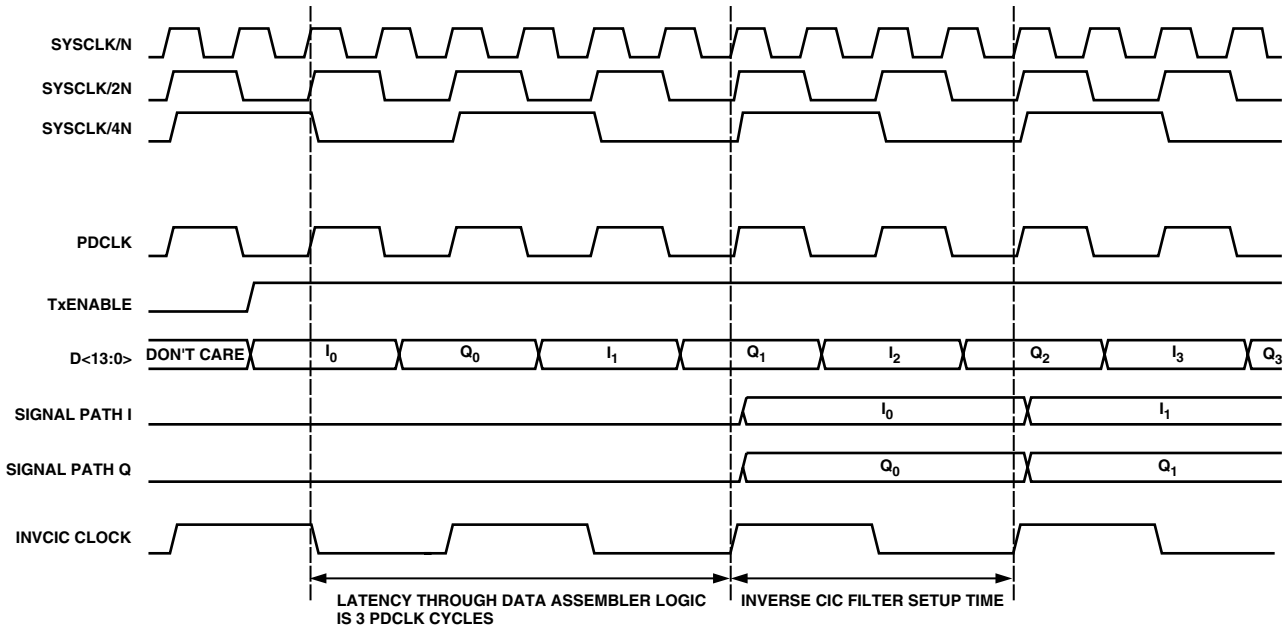


Figure 32. Latency from D<13:0> to Signal Processing Chain, Five PDCLK Cycles

EASE OF USE FEATURES

Profile Select

The profile select pins, PS0 and PS1, activate one of four internal profiles within the device. A profile is defined as a group of control registers. The AD9857 contains four identical register groupings associated with Profile 0, 1, 2, and 3. They are available to the user to provide rapid changing of device parameters via external hardware. Profiles are activated by simply controlling the logic levels on device pins P0 and P1 as defined in the table below.

Table VI. Profile Select Matrix

PS1	PS0	Profile
0	0	0
0	1	1
1	0	2
1	1	3

Each profile offers the following functionality:

1. Control of the DDS output frequency via the frequency tuning word
2. Control over the sum or difference of the quadrature modulator components via the Spectral Invert bit (only valid when the device is operating the Quadrature Modulation Mode)
3. Ability to bypass the Inverse CIC filter
4. Control of the CIC interpolation rate (1× to 63×), or bypass CIC Interpolator
5. Control of the output scale factor (which offers a gain range between 0 and 1.9921875)

The Profile Select Pins are sampled synchronously with the PDCLK signal for the Quadrature Modulation Mode and the Interpolating DAC Mode. For Single-Tone Mode they are sampled synchronously with SYSCLK (internal only).

Setting the Phase of the DDS

A feature unique to the AD9857 (versus previous ADI DDS products) is the ability for the user to preset the DDS accumulator to a value of 0. This sets the DDS outputs to sin = 0 and cos = 1. To accomplish this, the user simply programs a tuning word of 00000000h, which forces the DDS core to a "zero-phase" condition.

Reference Clock Multiplier

For DDS applications, the carrier is typically limited to about 40% of SYSCLK. For a 65 MHz carrier, the system clock required is above 160 MHz. To avoid the cost associated with high frequency references, and the noise coupling issues associated with operating a high-frequency clock on a PC board, the AD9857 provides an on-chip programmable clock multiplier that multiplies the Reference Clock frequency supplied to the part. The available clock multiplier range is from 4× to 20×, in integer steps. With the Reference Clock Multiplier enabled, the input reference clock required for the AD9857 can be kept in the 10 MHz to 50 MHz range for 200 MHz system operation, which results in cost and system implementation savings. The Reference Clock Multiplier function maintains clock integrity as evidenced by the system phase noise characteristics of the AD9857. External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 μF) provide the compensation zero for the REFCLK Multiplier PLL loop. The overall loop performance has been optimized for these component values.

Control of the PLL is accomplished by programming the 5-bit REFCLK Multiplier portion of Control Register 00h.

The PLL may be bypassed by programming a value of 01h. When bypassed, the PLL is shut down to conserve power.

When programmed for values ranging from 04h–14h (4–20 decimal), the PLL multiplies the REFCLK input frequency by the corresponding decimal value. The maximum output frequency of the PLL is restricted to 200 MHz. Whenever the PLL value is changed, the user should be aware that time must be allocated to allow the PLL to lock (approximately 1 ms). Indication of the PLL's lock status is provided externally via the PLL Lock Indicator pin.

PLL Lock (See Reference Clock Multiplier)

The PLL Lock indicator (PLL_LOCK) is an active high output pin, serving as a flag to the user that the device has locked to the REFCLK signal.

The status of the PLL Lock Indicator can be used to control some housekeeping functions within the device if the user sets the PLL Lock Control bit to 0 (Control Register 00h<5>). Assuming that the PLL Lock Control bit is cleared (Logic 0), the status of the PLL Lock Indicator pin has control over certain internal device functions. Specifically, if the PLL Lock Indicator is a Logic 0 (PLL *not* locked), then the following static conditions apply:

1. The accumulator in the DDS core is cleared.
2. The internal I and Q data paths are forced to a value of ZERO.
3. The CIC filters are cleared.
4. The PDCLK is forced to a Logic 0.
5. Activity on the TxENABLE pin is ignored.

On the rising edge of the PLL Lock Indicator the static conditions mentioned above are removed and the device assumes normal operation.

If the user requires the PDCLK to continue running, the PLL Lock Control bit (Control Register 00h<5>) can be set to a Logic 1. When the PLL Lock Control bit is set, the PLL lock indicator pin functionality remains the same, but the internal operations noted in 1 through 5 above will not occur. The default state of the PLL Lock Control bit is set, suppressing internal monitoring of the PLL lock condition.

Single or Differential Clock

In a noisy environment, a differential clock is usually considered superior in performance over a single-ended clock in terms of jitter performance, noise ingress, EMI, etc. However, sometimes it is desirable (economy, layout, etc.) to use a single-ended clock. The AD9857 allows the use of either a differential or single-ended Reference Clock input signal. A logic high on the DIFFCLKEN pin selects a differential clock input, whereas a logic low on this pin selects a single-ended clock input. If a differential clock is to be used, logic high is asserted on the DIFFCLKEN pin. The Reference Clock signal is applied to the REFCLK pin, and the inverted (complementary) Reference Clock signal is applied to $\overline{\text{REFCLK}}$. If a single-ended Reference Clock is desired, logic low should be asserted on the DIFFCLKEN pin, and the Reference Clock signal applied to REFCLK *only*. $\overline{\text{REFCLK}}$ is ignored in single-ended mode, and can be left floating or tied low.

CIC Overflow Pin

Any condition that leads to an overflow of the CIC filters will cause signal activity on the CIC_OVRFL pin. The CIC_OVRFL pin will remain low (Logic 0) unless an overflow condition occurs. When an overflow condition occurs, the CIC_OVRFL pin does not remain high, but will toggle in accordance with data going through the CIC filter.

Clearing the CIC Filter

The AD9857 CIC filter(s) can become corrupted if certain illegal (i.e., non-valid) operating conditions occur. If the CIC filter(s) become corrupted, invalid results will be apparent at the output and the CIC_OVRFL output pin will exhibit activity (toggling between Logic 0 and Logic 1 in accordance with the data going through the CIC filter). Examples of situations that may cause the CIC filter to produce invalid results include:

1. Transmitting data when the PLL is not locked to the reference frequency.
2. Operating the part above the maximum specified system clock rate (200 MHz).
3. Changing the CIC filter interpolation rate during transmission.

If the CIC filters become corrupted, the user can take advantage of the CIC Clear bit (Control Register 00h<7>) to easily clear the filter(s). By writing the CIC Clear bit to a Logic 1, the AD9857 enters a routine that clears the entire datapath, including the CIC filter(s). The routine simply ignores the D<13:0> pins and forces logical zeros on to the I and Q signal processing paths while holding the CIC filter memory elements reset. The routine is complete once all data path memory elements are cleared. The CIC clear bit is also reset, so that the user does not have to explicitly clear it.

NOTE: The time required to complete this routine is a function of clock speed *and* the overall interpolation rate programmed into the device. Higher interpolation rates create lower clock frequencies at the filters preceding the CIC filter(s), causing the routine time to increase.

In addition to the capability to detect and clear a corrupted CIC filter condition, there are several conditions within the AD9857 that cause an automatic datapath flush, which includes clearing the CIC filter. The following conditions automatically clear the signal processing chain of the AD9857:

1. Power-On Reset—Proper initialization of the AD9857 requires the Master Reset pin to be active high for at least 5 REFCLK clock cycles. After Master Reset becomes inactive, the AD9857 completes the datapath clear routine as described above.
2. PLL Not Locked To the Reference Clock—If the PLL Lock Control bit is cleared and the AD9857 detects that the PLL is not locked to the reference clock input, the AD9857 invokes and completes the datapath clear routine after lock has been detected. When the PLL Lock Control bit is set, the datapath clear routine will not be invoked if the PLL is not locked. The PLL Lock Control bit is set upon initialization, disabling the clear routine functionality due to the PLL.
3. Digital Power-Down—When the DPD pin is driven high, the AD9857 will automatically invoke and complete the datapath clear routine before powering down the digital section.
4. Full Sleep Mode—If the sleep mode control bit is set high, the AD9857 will automatically invoke and complete the datapath clear routine before powering down.

Digital Power-Down

The AD9857 includes a digital power-down feature that can be hardware- or software-controlled. Digital power-down allows the users to save considerable operating power (60–70% reduction) when not transmitting and requires no "startup" time before the next transmission can occur. The digital power-down feature is ideal for burst mode applications where fast "begin to transmit" time is required.

During digital-power down the internal clock synchronization is maintained and the PDCLK output continues to run. Reduction in power is achieved by stopping many of the internal clocks that drive the signal processing chain.

Invoking the Digital Power-Down causes supply current transients. Therefore, some users may not want to invoke the DPD function in order to ease power supply regulation considerations.

Hardware-Controlled Digital Power-Down

The hardware-controlled method for reducing power is to apply a Logic 1 to the DPD pin. Restarting the part after a Digital Power-Down is accomplished by applying a logic zero to the DPD pin. The DPD pin going to Logic 0 can occur simultaneously with the activation of TxENABLE.

The user will notice some time delay between invoking the digital power-down function and the actual reduction in power. This is due to an automatic routine that clears the signal processing chain before stopping the clocks. Clearing the signal processing chain before powering down ensures that the AD9857 is ready to transmit when Digital Power-Down mode is deactivated (see the Clearing the CIC Filter section for details).

Software-Controlled Digital Power-Down

The software-controlled method for reducing digital power between transmissions is simply an enable or disable of an automatic power-down function. When enabled, digital power-down between bursts occurs automatically after all data has passed the AD9857 signal processing path.

When the AD9857 senses the TxENABLE input indicates the end of a transmission, an on-chip timer is used to verify that the data has completed transmission before stopping the internal clocks that drive the signal processing chain memory elements. As with the hardware activation method, clock synchronization is maintained and the PDCLK output continues to run. An active high signal on TxENABLE automatically restarts the internal clocks, allowing the next burst transmission to start immediately.

The automatic digital power-down between bursts is enabled by writing the Control Register 01h<2> bit high. Writing the Control Register 01h<2> bit low will disable the function.

Full Sleep Mode

When coming out of Full Sleep Mode, it is necessary to wait for the PLL Lock Indicator to go high. Full Sleep Mode functionality is provided by programming one of the Control Registers (01h<3>). When the Full Sleep bit is set to a Logic 1, the device shuts down both its digital and analog sections. During Full Sleep Mode, the contents of the registers of the AD9857 are maintained. This mode yields the minimum possible device power dissipation.

Power Management Considerations

The thermal impedance for the AD9857 80-lead LQFP package is θ_{JA} = 35°C/W. The maximum allowable power dissipation using this value is calculated using $\Delta T = P \times \theta_{JA}$.

$$P = \frac{\Delta T}{\theta_{JA}}$$

$$P = \frac{150 - 85}{35}$$

$$P = 1.85\,W$$

The AD9857 power dissipation is at or below this value when the SYSCLK frequency is at 200 MHz or lower with all optional features enabled. The maximum power dissipation occurs while operating the AD9857 as a quadrature modulator at the maximum system clock frequency with TxENABLE in a logic high state 100% of the time the device is powered. Under these conditions the device operates with all possible circuits enabled at maximum speed.

Significant power saving may be seen by using a TxENABLE signal that toggles low during times when the device does not modulate.

The thermal impedance of the AD9857 package was measured in a controlled temperature environment at temperatures ranging from 28°C to 85°C with no air flow. The device under test was soldered to an AD9857 evaluation board and operated under conditions that generate maximum power dissipation. The thermal resistance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance of a package is determined by package material and its physical dimensions. The dissipation of the heat from the package is directly dependent upon the ambient air conditions and the physical connection made between the IC package and the PCB. Adequate dissipation of power from the AD9857 relies upon all power and ground pins of the device being soldered directly to copper planes on a PCB.

Many variables contribute to the operating junction temperature within a device. They include:

1. Package Style
2. Selection Mode of Operation
3. Internal System Clock Speed
4. Supply Voltage
5. Ambient Temperature

The power dissipation of the AD9857 in a given application is determined by several operating conditions. Some of these conditions, such as supply voltage and clock speed, have a direct relationship with power dissipation. The most important factors affecting power dissipation are the following:

Supply Voltage

This affects power dissipation and junction temperature since power dissipation equals supply voltage multiplied by supply current. It is recommended that the user design for a 3.3 V nominal supply voltage in order to manage the affect of supply voltage on the junction temperature of the AD9857.

Clock Speed

This directly and linearly influences the total power dissipation of the device and, therefore, junction temperature. As a rule, the user should always select the lowest internal clock speed possible to support a given application to minimize power dissipation. Normally, the usable frequency output bandwidth from a DDS is limited to 40% of the system clock rate to keep reasonable requirements on the output low-pass filter. This means that for the typical DDS application, the system clock frequency should be 2.5 times the highest output frequency.

Mode of Operation

The AD9857 has three modes of operation that consume significantly different amounts of power. When operating in the Quadrature Modulation Mode, the AD9857 will dissipate about twice the power as when operating as a single-tone DDS. When operating as a quadrature modulator, the AD9857 has features that facilitate power management tactics. For example, the TxENABLE pin may be used in conjunction with the auto power-down bit to frame bursts of data and automatically switch the device into a low-power state when there is no data to be modulated.

Equivalent I/O Circuits

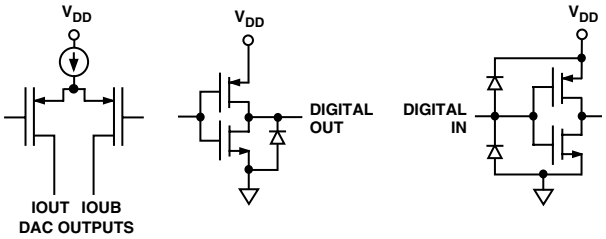
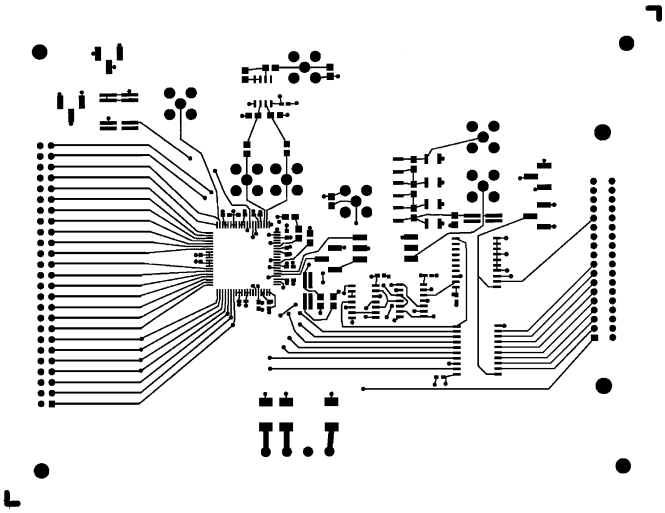
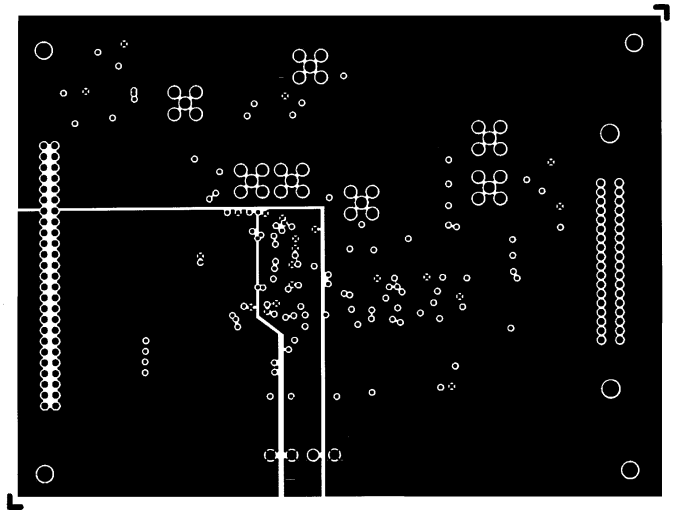


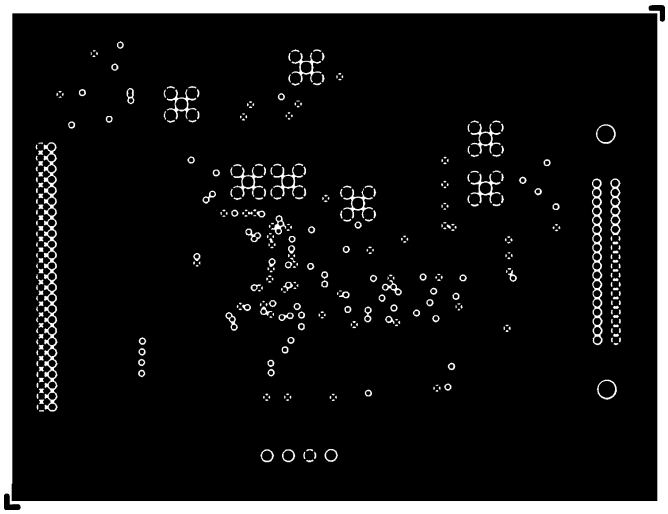
Figure 33. Equivalent I/O Circuits



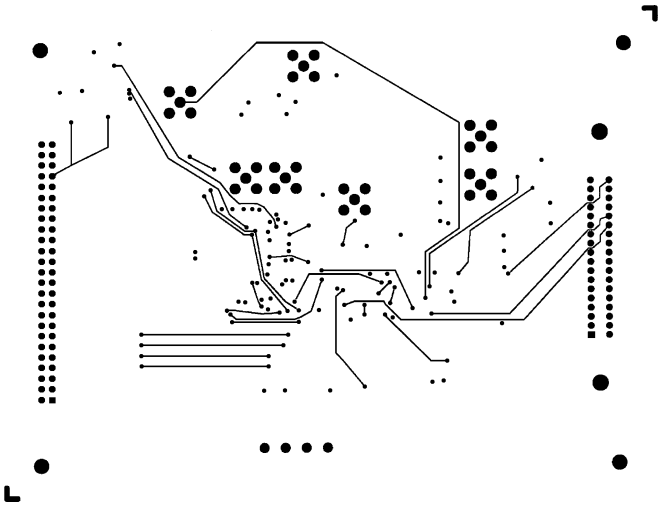
A. Top View



C. Power Plane



B. Ground Plane



D. Bottom View

Figure 34. Application–Example Circuits

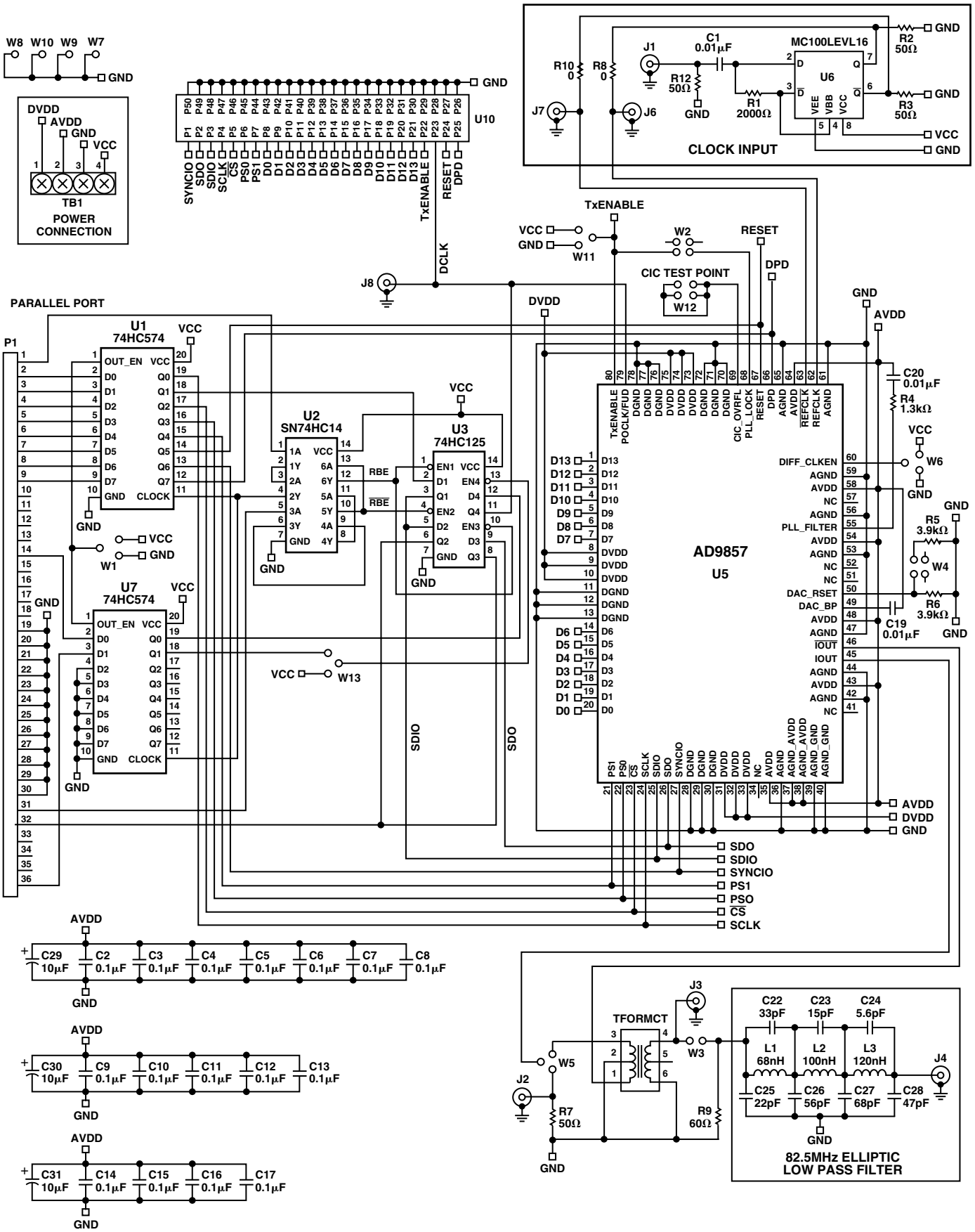
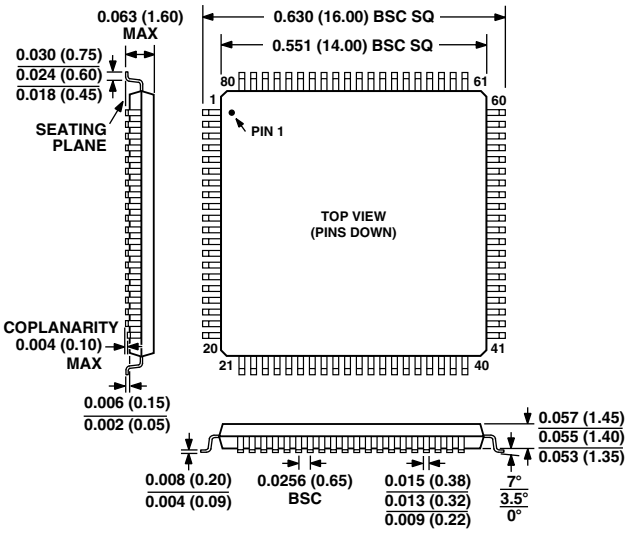


Figure 35. Schematic of AD9857 Evaluation PCB

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Lead Quad Flatpack (ST-80)



CONTROLLING DIMENSIONS IN MILLIMETERS.
CENTER FIGURES ARE NOMINAL UNLESS OTHERWISE NOTED.

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